

CBT (5-V) and CBTLV (3.3-V) Bus Switches



December 1998

Logic Products

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CBT (5-V) and CBTLV (3.3-V) Bus Switches Data Book







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INTRODUCTION

The CBT (5-V) and CBTLV (3.3-V) Bus Switches Data Book includes a comprehensive listing of the industry's standard for bus-switch technology, product offerings, and availability. These devices provide isolation when the switch is open and near-zero propagation delay when the switch is closed. Texas Instruments (TI[™]) bus switches provide ideal solutions for bus isolation, bus exchanging, memory interleaving, voltage translation, and docking support.

The CBTLV family is TI's new growing line of 3.3-V bus switches. Low-voltage bus switches allow for design ease in a low-voltage environment. Low voltage also means low power consumption – a key careabout for any battery-powered system.

TI's line of 5-V bus switches, the CBT family, is larger than ever. With single-gate devices, devices with integrated diodes, and Widebus[™] devices available, the CBT bus-switch family offers a complete 5-V bus-switch portfolio.

TI's bus switches include 1-, 2-, 4-, 8-, 10-, 16-, 18-, 20-, and 24-bit solutions. CBT and CBTLV bus switches are designed to match the input/output combinations of traditional logic devices.

For more information on these products, including availability and pricing, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI home page at http://www.ti.com/sc/logic.

For a listing of TI logic products, please order the *Logic CD-ROM* (literature number SCBC001) or *Logic Selection Guide* (literature number SDYU001) by calling the literature response center at 1-800-477-8924.

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Example:



1 Standard Prefix

Example: SN - Standard Prefix

- 2 Temperature Range
- Examples: 54 Military

74 – Commercial

3 Family

Examples: Blank - Transistor-Transistor Logic ABT – Advanced BiCMOS Technology ABTE - Advanced BiCMOS Technology/ Enhanced Transceiver Logic AC/ACT - Advanced CMOS Logic AHC/AHCT - Advanced High-Speed CMOS Logic ALB - Advanced Low-Voltage BiCMOS ALS - Advanced Low-Power Schottky Logic ALVC - Advanced Low-Voltage CMOS Technology AS - Advanced Schottky Logic BCT - BiCMOS Bus-Interface Technology CBT - Crossbar Technology CBTLV - Low-Voltage Crossbar Technology F – F Logic FB - Backplane Transceiver Logic/Futurebus+ GTL - Gunning Transceiver Logic HC/HCT - High-Speed CMOS Logic HSTL - High-Speed Transceiver Logic LS - Low-Power Schottky Logic LV - Low-Voltage CMOS Technology LVC - Low-Voltage CMOS Technology LVT - Low-Voltage BiCMOS Technology S – Schottky Logic SSTL - Stub Series-Terminated Logic

4 Special Features

Examples: Blank = No Special Features

- D Level-Shifting Diode (CBTD)
- H Bus Hold (ALVCH)
- R Damping Resistor on Inputs/Outputs (LVCR)
- S Schottky Clamping Diode (CBTS)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals

- 1G Single Gate
- 8 Octal IEEE Std 1149.1 (JTAG)
- 16 Widebus™ (16, 18, and 20 bit)
- 18 Widebus IEEE Std 1149.1 (JTAG)
- 32 Widebus+™ (32 and 36 bit)

6 **Options**

Examples: Blank = No Options 2 – Series-Damping Resistor on Outputs 4 – Level Shifter $25 - 25-\Omega$ Line Driver

7 Function

Examples: 244 – Noninverting Buffer/Driver 374 – D-Type Flip-Flop 573 – D-Type Transparent Latch 640 – Inverting Transceiver

8 Device Revision

Examples: Blank = No Revision Letter Designator A–Z

9 Packages

Examples: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DBQ, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBV, DCK – Small-Outline Transistor Package (SOT)
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FK – Leadless Ceramic Chip Carrier (LCCC)
FN – Plastic Leaded Chip Carrier (PLCC)
GB – Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV – Ceramic Quad Flat Package (CQFP)
J, JT – Ceramic Dual-In-Line Package (CDIP)
N, NP, NT – Plastic Dual-In-Line Package (PDIP)
PAG, PAH, PCA, PCB, PM, PN, PZ –
Thin Quad Flat Package (TQFP)
PH, PQ, RC – Quad Flat Package (QFP)
W, WA, WD – Ceramic Flat Package (CFP)

10 Tape and Reel

All new or changed devices in the DB and PW package types include the R designation for reeled product. Existing products designated as LE presently maintain that designation, but will be converted to R in the future.

Nomenclature Examples:

- For an Existing Device SN74LVTxxxDBLE For a New or Changed Device – SN74LVTxxxADBR
- LE Left Embossed (valid for DB and PW packages only) R – Standard (valid for all surface-mount packages except
- existing DB and PW devices)
- There is no functional difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.



NOTIFICATION OF PACKAGE NOMENCLATURE ALIAS (for Standard Linear and Logic device names of greater than 18 characters)

TI is converting from its current order-entry system to a more advanced system. This conversion requires modifications, both internal and external, to TI's current business processes. This new system will ultimately provide significant improvements to all facets of TI's business – from production, to order entry, to logistics. One change required is a limitation of TI part numbers to no more than 18 characters in length. Based on customer inputs, Standard Linear and Logic determined the least disruptive implementations as outlined below:

1. Package alias

TI will use a package alias to denote specific package types for devices currently exceeding 18 characters in length. Table 1 shows a mapping of package codes to an alias single-character representation.

CURRENT PACKAGE CODE	ALIAS	
DL	L	
DGG/DBB	G	
DGV	V	
DLR	LR – tape/reel packing	
DGGR/DBBR	GR - tape/reel packing	
DGVR	VR - tape/reel packing	

Table 1

Current: SN74 ALVCH 162269A DGGR New: SN74 ALVCH 162269A GR

2. Resistor-option nomenclature

For devices greater than 18 characters with input and output resistors, TI will adopt a simplified nomenclature to designate the resistor option. This will eliminate the redundant "2" (designating output resistors) when the part number also contains an "R" (designating input/output resistors).



There is no change to the device or data-sheet electrical parameters. The packages involved and the changes in nomenclature are noted in Table 1.

These nomenclature changes are being gradually implemented. The first customer-visible conversions for TI logic devices will be made to data sheets. Over the next few months, TI logic data sheets will be updated. These changes in device nomenclature do not reflect a change in device performance or process characteristics.



INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

Ci	Input capacitance The internal capacitance at an input of the device	
C _{io}	Input/output capacitance Input-to-output internal capacitance; transcapacitance	
Co	Output capacitance The internal capacitance at an output of the device	
C _{pd}	Power dissipation capacitance Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$	
f _{max}	Maximum clock frequency The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification	
I _{BHH}	Bus-hold high sustaining current The sourcing current of the bus-hold circuit to maintain the input at or above the minimum V_{IH} , if the last valid logic state at the input was a high	
І _{ВННО}	Bus-hold high overdrive current The current required to overcome the sourcing current of the bus-hold circuit and switch the input to a low state	
I _{BHL}	Bus-hold low sustaining current The sinking current of the bus-hold circuit to maintain the input at or below the maximum V_{IL} , if the last valid logic state at the input was a low	
IBHLO	Bus-hold low overdrive current The current required to overcome the sinking current of the bus-hold circuit and switch the input to a high state	
ICC	Supply current The current into* the V_{CC} supply terminal of an integrated circuit	
∆ICC	Supply current change The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}	
ICEX	Output high leakage current The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_0 = 5.5 V$	

*Current out of a terminal is given as a negative value.



GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

l _{l(hold)}	Input hold current Input current that holds the input at the previous state when the driving device goes to a		
	high-impedance state		
IIH	High-level input current		
	The current into* an input when a high-level voltage is applied to that input		
Ι _{ΙL}	Low-level input current		
	The current into* an input when a low-level voltage is applied to that input		
l _{off}	Input/output power-off leakage current The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC} = 0$ V		
юн	High-level output current		
•	The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output		
l _{OL}	Low-level output current		
	The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output		
loz	Off-state (high-impedance-state) output current (of a 3-state output)		
	The current that flows through the output gates when the device is in the high-impedance state		
I _{OZPD}	Power-down (high-impedance-state) output current (of a 3-state output)		
	The current that flows into or out of the output stage when the device is being powered down from the high-impedance state		
IOZPU	Power-up (high-impedance-state) output current (of a 3-state output)		
	The current that flows into or out of the output stage when the device is being powered up from high-impedance state		
t _a Access time			
	The time interval between the application of a specified input pulse and the availability of valid signals at an output		
t _c	Clock cycle time		
	Clock cycle time is 1/f _{max} .		
t _{dis}	Disable time (of a 3-state or open-collector output)		
	The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state		
	NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.		
t _{en}	Enable time (of a 3-state or open-collector output)		
	The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)		
	NOTE: In the case of memories, this is the access time from an enable input (e.g., \overline{OE}). For 3-state outputs, t _{en} = t _{PZH} or t _{PZL} . Open-collector outputs change only if they are responding to data that would cause the output to go low, so t _{en} = t _{PHL} .		

*Current out of a terminal is given as a negative value.



th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

tpd Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

tPLH Propagation delay time, low-to-high level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} Disable time (of a 3-state output) from low level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} Enable time (of a 3-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} Enable time (of a 3-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{sk(o)} Output skew

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.



t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.

tw Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

$\Delta t / \Delta v$ Input voltage transition rate

The input transition rise or fall rate corresponding to the change in signal amplitude with time

$\Delta t / \Delta V_{CC}$ Power supply power-up rate

The power-up ramp rate corresponds to the transition rate of the supply voltage when the device is being powered up.

V_{IH} High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

VIL Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

V_{OL} Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

VIT+ Positive-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT-}

VIT- Negative-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}



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SN74CBT1G125 SINGLE FET BUS SWITCH

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5 VCC

4 || B

DBV OR DCK PACKAGE (TOP VIEW)

OE

A 🛛 2

GND 3

- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Small-Outline Transistor (DBV, DCK) Packages

description

The SN74CBT1G125 features a single high-speed line switch. The switch is disabled when the output-enable $\overline{(OE)}$ input is high.

The SN74CBT1G125 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE	
INPUT OE FUNCTION	
L	A port = B port
Н	Disconnect

ELINCTION TABLE

logic diagram (positive logic)





2-3

SN74CBT1G125 SINGLE FET BUS SWITCH

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	\ldots –0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	
Package thermal impedance, θ_{JA} (see Note 2): DBV package	
DCK package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	I _I = -18 mA					-1.2	V
Ц		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$					±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or G	ND			1	μA
Ci	Control input	V _I = 3 V or 0					3		pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$				4		pF
r _{on} §		$V_{CC} = 4 V,$	TYP at V _{CC} = 4 V,	V _I = 2.4 V,	lj = 15 mA		14	20	
			$V_{i} = 0$	lj = 64 mA			5	7	0
		V _{CC} = 4.5 V	VI = 0	lı = 30 mA			5	7	52
			$V_{I} = 2.4 V,$	lj = 15 mA			10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPLIT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT	
		(001101)	MIN M	IAX	MIN	MAX		
t _{pd} ¶	A or B	B or A	C).35		0.25	ns	
^t en	ŌĒ	A or B		5.5	1.6	4.9	ns	
^t dis	ŌĒ	A or B		4.5	1	4.2	ns	

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBT1G125 SINGLE FET BUS SWITCH

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PARAMETER MEASUREMENT INFORMATION

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
 - D. The output is measured with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



- SN74CBTD1G125 SINGLE FET BUS SWITCH WITH LEVEL SHIFTING SCDS063B - JULY 1998 - REVISED OCTOBER 1998 **5-**Ω Switch Connection Between Two Ports **DBV OR DCK PACKAGE** (TOP VIEW) **TTL-Compatible Control Input Levels Packaged in Plastic Small-Outline** OE 5 VCC Transistor (DBV, DCK) Packages
- description

The SN74CBTD1G125 features a single high-speed line switch. The switch is disabled when the output-enable $\overline{(OE)}$ input is high. A diode to V_{CC} is integrated on the chip to allow for level shifting between 5-V inputs and 3.3-V outputs.

ΑŪ 2

3

4 || B

GND

The SN74CBTD1G125 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE				
	FUNCTION			
L	A port = B port			
н	Disconnect			

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	\ldots -0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	347°C/W
DCK package	389°C/W
Storage temperature range, T _{stg}	. –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
∨ _{IH}	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
VOH		See Figure 2						
l		V _{CC} = 5.5 V,	V _I = 5.5 V or GND				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			1	μA
Ci	Control input	V _I = 3 V or 0						pF
C _{io(OFF}	=)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
r _{on} §		V _{CC} = 4.5 V	$\lambda = 0$	lj = 64 mA				
			VI = 0	lj = 30 mA				Ω
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} ¶	A or B	B or A		ns
^t en	ŌĒ	A or B		ns
^t dis	ŌĒ	A or B		ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).





PARAMETER MEASUREMENT INFORMATION

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns.
 - D. The output is measured with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





TYPICAL CHARACTERISTICS



SN74CBTS1G125 SINGLE FET BUS SWITCH

SCDS064A - JULY 1998 - REVISED OCTOBER 1998

5 🛛 V_{CC}

4 🛛 B

DBV OR DCK PACKAGE (TOP VIEW)

OE

GND 3

A 🛛 2

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Packaged in Plastic Small-Outline Transistor (DBV, DCK) Packages

description

The SN74CBTS1G125 features a single high-speed line switch with Schottky diodes on the I/O to clamp undershoot. The switch is disabled when the output-enable (\overline{OE}) input is high.

The SN74CBTS1G125 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE					
	FUNCTION				
L	A port = B port				
н	Disconnect				

logic diagram (positive logic)





SN74CBTS1G125 SINGLE FET BUS SWITCH

SCDS064A – JULY 1998 – REVISED OCTOBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Package thermal impedance, θ_{JA} (see Note 2): DBV package .	
DCK package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-0.7	V
1.	۱ _{IL}		V _I = GND				-1	μA
1]	ΙΗ	vCC = 2.2 v	VI = 5.5 V				50	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μΑ
Ci	Control input	$V_{ } = 3 V \text{ or } 0$						pF
C _{io(OFF)}		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
r _{on} §		$V_{CC} = 4 V,$	TYP at V _{CC} = 4 V,	$V_{I} = 2.4 V$, $I_{I} = 15 mA$				
			V _I = 0	l _l = 64 mA				0
		V _{CC} = 4.5 V		Ij = 30 mA				52
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at $V_{CC} = 5 V$ (unless otherwise noted), $T_A = 25^{\circ}C$.

S Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBTS1G125 SINGLE FET BUS SWITCH

SCDS064A - JULY 1998 - REVISED OCTOBER 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A					ns
ten	ŌĒ	A or B					ns
t _{dis}	OE	A or B					ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The output is measured with one input transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{P7I} and t_{P7H} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBT1G384 SINGLE FET BUS SWITCH

SCDS065A - JULY 1998 - REVISED OCTOBER 1998

5 VCC

4 🛛 OE

DBV OR DCK PACKAGE (TOP VIEW)

А

GND

В 🛛 2

3

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Packaged in Plastic Small-Outline Transistor (DBV, DCK) Packages

description

The SN74CBT1G384 features a single high-speed line switch. The switch is disabled when the output-enable (\overline{OE}) input is high.

The SN74CBT1G384 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE		
	FUNCTION	
L	A port = B port	
Н	Disconnect	

logic diagram (positive logic)





SN74CBT1G384 SINGLE FET BUS SWITCH

SCDS065A - JULY 1998 - REVISED OCTOBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Package thermal impedance, θ_{JA} (see Note 2): DBV package .	
DCK package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
∨ _{IH}	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDI	TIONS		MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = –18 mA					-1.2	V
Ι		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$					±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or G	ND			1	μA
Ci	Control input	V _I = 3 V or 0							pF
C _{io(OFF}	=)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$						pF
		$V_{CC} = 4 V,$	TYP at $V_{CC} = 4 V$,	V _I = 2.4 V,	lı = 15 mA				
- 8			V/- 0	lj = 64 mA					0
¹ on ³		V _{CC} = 4.5 V	VI = 0	l _l = 30 mA					52
			$V_{I} = 2.4 V,$	lj = 15 mA					

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC} :	= 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
^t en	OE	A or B					ns
^t dis	ŌĒ	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBT1G384 SINGLE FET BUS SWITCH

SCDS065A - JULY 1998 - REVISED OCTOBER 1998



PARAMETER MEASUREMENT INFORMATION

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The output is measured with one input transition per measurement.
 - E. $t_{PI 7}$ and t_{PH7} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as t_{en} .
 - G. tpLH and tpHL are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



 SN74CBTD1G384 SINGLE FET BUS SWITCH WITH LEVEL SHIFTING SCDS066B – JULY 1998 – REVISED OCTOBER 1998
 5-Ω Switch Connection Between Two Ports
 TTL-Compatible Control Input Levels
 Packaged in Plastic Small-Outline Transistor (DBV, DCK) Packages
 A [1 5] 2

description

The SN74CBTD1G384 features a single high-speed line switch. The switch is disabled when the output-enable (\overline{OE}) input is high. A diode to V_{CC} is integrated on the chip to allow for level shifting between 5-V inputs and 3.3-V outputs.

GND

3

4 🛛 OE

The SN74CBTD1G384 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE		
	FUNCTION	
L	A port = B port	
н	Disconnect	

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Package thermal impedance, θ_{JA} (see Note 2): DBV package	
DCK package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
∨ _{IH}	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CONDITI	TEST CONDITIONS		TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA				-1.2	V
VOH		See Figure 2						
l		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	l _O = 0,	$V_I = V_{CC}$ or GND			1	μA
Ci	Control input	V _I = 3 V or 0						pF
C _{io(OFF}	=)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
			$\lambda = 0$	lj = 64 mA				
r _{on} §		V _{CC} = 4.5 V	VI=0	lj = 30 mA				Ω
			$V_{I} = 2.4 V,$	lj = 15 mA				

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} ¶	A or B	B or A		ns
^t en	ŌĒ	A or B		ns
^t dis	ŌĒ	A or B		ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).





PARAMETER MEASUREMENT INFORMATION

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns.
 - D. The output is measured with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as t_{en} .
 - G. tpLH and tpHL are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms





TYPICAL CHARACTERISTICS



SN74CBTS1G384 SINGLE FET BUS SWITCH

SCDS067A - JULY 1998 - REVISED OCTOBER 1998

5 🛛 V_{CC}

4 🛛 OE

DBV OR DCK PACKAGE (TOP VIEW)

A

GND

В 🛛 2

3

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Packaged in Plastic Small-Outline Transistor (DBV, DCK) Packages

description

The SN74CBTS1G384 features a single high-speed line switch with Schottky diodes on the I/O to clamp undershoot. The switch is disabled when the output-enable (\overline{OE}) input is high.

The SN74CBTS1G384 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE			
	FUNCTION		
L	A port = B port		
н	Disconnect		

logic diagram (positive logic)





SN74CBTS1G384 SINGLE FET BUS SWITCH

SCDS067A - JULY 1998 - REVISED OCTOBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Package thermal impedance, θ_{JA} (see Note 2): DBV package	
DCK package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT	
VIK		$V_{CC} = 4.5 V,$	l _l = –18 mA				-0.7	V	
II	۱ _{IL}	V _{CC} = 5.5 V	$V_{I} = GND$				-1	μA	
	ΙΗ		VI = 5.5 V				50	μA	
ICC		V _{CC} = 5.5 V,	IO = 0,	VI = V _{CC} or GND			3	μA	
Ci	Control input	V _I = 3 V or 0						pF	
C _{io(OFF}	=)	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF	
		$V_{CC} = 4 V,$	TYP at V _{CC} = 4 V,	$V_{I} = 2.4 V$, $I_{I} = 15 mA$					
- 8			$\lambda t = 0$	l _l = 64 mA				Ω	
ons	$V_{CC} = 4$	V _{CC} = 4.5 V	V] = 0	Ij = 30 mA					
			V _I = 2.4 V,	lj = 15 mA					

[‡] All typical values are at $V_{CC} = 5 V$ (unless otherwise noted), $T_A = 25^{\circ}C$.

S Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.


SN74CBTS1G384 SINGLE FET BUS SWITCH

SCDS067A - JULY 1998 - REVISED OCTOBER 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO V _{CC} = 4		= 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
		(001101)	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A					ns
^t en	ŌĒ	A or B					ns
t _{dis}	OE	A or B					ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 Winsert and a supplied by a supplied by a supplied by a supplied by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The output is measured with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tPZL and tPZH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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SN74CBT3125 QUADRUPLE FET BUS SWITCH

14 🛛 V_{CC}

13 40E

SCDS021E - MAY 1995 - REVISED MAY 1998

- Standard '125-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3125 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (\overline{OE}) input is high.

The SN74CBT3125 is characterized for operation from -40° C to 85° C.



	FUNCTION
L	A port = B port
н	Disconnect

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, and PW packages.

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1B [2OE [2A [2B [3 4 5 6	12] 4A 11] 4B 10] 3OE 9] 3A
GND	7	8 🛛 3B
DE	BQ PAC	KAGE EW)
NC [$_{1}$ U	
	2	15 40E
1A [3	14 🛛 4A
1B [4	13 🛛 4B
2 <mark>0E</mark>	5	12 30E
~ ~ F		

D, DB, DGV, OR PW PACKAGE (TOP VIEW)

1OF

1A 🛛 2

NC - No internal connection

2B 🛛 7

GND

10 3B

9 NC

SN74CBT3125 QUADRUPLE FET BUS SWITCH

SCDS021E - MAY 1995 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		0.5 V to 7 V 0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{K} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	127°C/W
	DB package	158°C/W
	DBQ package	139°C/W
	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT	
VIK		$V_{CC} = 4 V,$	l _l = –18 mA				-1.2	V
lj		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0				3		pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			4		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lı = 15 mA		16	22	
r _{on} ¶			V _I = 0	lı = 64 mA		5	7	Ω
		V _{CC} = 4.5 V		lı = 30 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.



SN74CBT3125 QUADRUPLE FET BUS SWITCH

SCDS021E - MAY 1995 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTPUT)	V _{CC} = 4	v	= V _{CC} ± 0.	= 5 V 5 V	UNIT
		(0011 01)	MIN M	АХ	MIN	MAX	
t _{pd} †	A or B	B or A	C	.35		0.25	ns
ten	ŌĒ	A or B		6	1.6	5.4	ns
tdis	ŌĒ	A or B		5.1	1	4.7	ns

[†]The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tPLZ and tPHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBT3126 QUADRUPLE FET BUS SWITCH

SCDS020E - MAY 1995 - REVISED MAY 1998

- Standard '126-Type Pinout (D, DGV, and PW Packages)
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

The SN74CBT3126 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
L	Disconnect
н	A = B

logic diagram (positive logic)

D, DGV, C	OR PW PACKAGE
(T	OP VIEW)
1OE [1	14 V _{CC}
1A [2	13 4OE
1B [3	12 4A
2OE [4	11 4B
2A [5	10 3OE
2B [6	9 3A
GND [7	8 3B
DBC	PACKAGE
(T	OP VIEW)
NC [1	16 V _{CC}
1OE [2	15 40E
1A [3	14 4A
1B [4	13 4B
2OE [5	12 30E
2A [6	11 3A
2B [7	10 3B
GND [8	9 NC

NC - No internal connection



Pin numbers shown are for the D, DGV, and PW packages.

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SN74CBT3126 QUADRUPLE FET BUS SWITCH

SCDS020E - MAY 1995 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		–0.5 V to 7 V –0.5 V to 7 V 128 mA
Input clamp current $l_{\mathcal{L}}(V_{\mathcal{L}} < 0)$		-50 mA
Package thermal impedance. θ_{1A} (see Note 2):	D package	127°C/W
·	DBQ package	139°C/W
	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
VIK		$V_{CC} = 4 V,$	lı = –18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	VI = V _{CC} or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				3		pF
Cio(OFF)		$V_{O} = 3 V \text{ or } 0,$	OE = GND			4		pF
		$V_{CC} = 4 V,$	TYP at V_{CC} = 4 V,	V _I = 2.4 V, I _I = 15 mA		16	22	
r _{on} ¶			$\lambda = 0$	lj = 64 mA		5	7	0
		V _{CC} = 4.5 V	VI = 0	lj = 30 mA		5	7	52
			$V_{1} = 2.4 V,$	l _l = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBT3126 QUADRUPLE FET BUS SWITCH

SCDS020E - MAY 1995 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTPUT)	V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT	
			MIN MAX	MIN	MAX		
t _{pd} †	A or B	B or A	0.35		0.25	ns	
ten	OE	A or B	5.4	1.6	5.1	ns	
^t dis	OE	A or B	5	1	4.5	ns	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH andtpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS001H - NOVEMBER 1992 - REVISED MAY 1998

 Functionally Equivalent to QS3244 Standard '244-Type Pinout 	DB, DBQ, DGV, DW, OR PW PACKAG (TOP VIEW)				
 5-Ω Switch Connection Between Two Ports 					
TTL-Compatible Input Levels					
Package Options Include Plastic	2B4 🛛 3 18 🗋 1B1				
Small-Outline (DW), Shrink Small-Outline	1A2 4 17 2A4				
(DB, DBQ), Thin Very Small-Outline (DGV),	2B3 🛛 5 16 🗍 1B2				
and Thin Shrink Small-Outline (PW)	1A3 🛛 6 🛛 15 🗍 2A3				
Packages	2B2 🚺 7 14 🗍 1B3				
-	1A4 🚺 8 13 🗍 2A2				
description	2B1 🚺 9 12 🗍 1B4				
The SN74CBT3244 provides eight bits of	GND [10 11] 2A1				

The SN74CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3244 is characterized for operation from 0°C to 70 °C.

FUNCTION TABLE (each 4-bit bus switch)

	FUNCTION
L	A port = B port
Н	Disconnect

logic diagram (positive logic)



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SCDS001H - NOVEMBER 1992 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5 V to 7 V
Continuous channel current		128 mA
Clamp current, I_{K} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	115°C/W
	DBQ package	118°C/W
	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±5	μA
ICC		V _{CC} = 5.5 V,	lO = 0,	$V_I = V_{CC}$ or GND			50	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
Ci	Control inputs	V _I = 3 V or 0				3		pF
Cio(OFF	=)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$			6		pF
			$\lambda = 0$	l _l = 64 mA		5	7	
ron¶		$V_{CC} = 4.5 V$	VI=0	lı = 30 mA		5	7	Ω
			V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25° C.

 \S This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



SCDS001H - NOVEMBER 1992 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} †	A or B	B or A		0.25	ns
^t en	ŌE	A or B	1	8.9	ns
^t dis	ŌĒ	A or B	1	7.4	ns

[†]This propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PI7} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tPLH andtPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS079 - JULY 1998

 Functionally Equivalent to QS3244 Standard '244-Type Pinout 	DB, DBQ, DGV, DW, OR PW PACKAG (TOP VIEW)		
 25-Ω Switch Connection Between Two Ports 		1 20 2 19] V _{CC}] 20E
TTL-Compatible Input Levels	2B4 🖸	3 18] 1B1
 Package Options Include Plastic 	1A2 🛛 4	4 17	2A4
Small-Outline (DW), Shrink Small-Outline	2B3 🛛 🕯	5 16] 1B2
(DB, DBQ), Thin Very Small-Outline (DGV),	1A3 🛛 🤅	6 15	2A3
and Thin Shrink Small-Outline (PW)	2B2 🛛 7	7 14] 1B3
Packages	1A4 🛛 १	8 13] 2A2
	2B1 🛛 🤅	9 12] 1B4
description		10 11] 2A1

The SN74CBTR3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The device has equivalent $25 \cdot \Omega$ series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.

The SN74CBTR3244 is characterized for operation from 0°C to 70 °C.

(each 4-bit bus switch)				
	FUNCTION			
L	A port = B port			
н	Disconnect			

S. When e switch need for **BREVIEW**

FUNCTION TABLE each 4-bit bus switch)



SCDS079 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Clamp current, $I_K (V_{I/O} < 0)$		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	115°C/W
	DBQ package	118°C/W
	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T _{sta}	•••••	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCDS079 - JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER		TEST CONDIT	IONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±5	μA
ICC		V _{CC} = 5.5 V,	IO = 0,	$V_I = V_{CC}$ or GND			50	μA
∆lcc [‡]	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{io(OFF}	=)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
			$\lambda = 0$	lj = 64 mA				
r _{on} §		V _{CC} = 4.5 V	V] = 0	lı = 30 mA				Ω
			V _I = 2.4 V,	l _l = 15 mA				

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} ¶	A or B	B or A		ns
ten	ŌĒ	A or B		ns
tdis	ŌĒ	A or B		ns

This propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS079 - JULY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH andtPHL are the same as tpd.





SCDS002J - NOVEMBER 1992 - REVISED MAY 1998

DB, DBQ, DGV, DW, OR PW PACKAGE Functionally Equivalent to QS3245 (TOP VIEW) Standard '245-Type Pinout **5-**Ω Switch Connection Between Two Ports NC 20 IV_{CC} **TTL-Compatible Input Levels** 19 0E A1 L 2 18 B1 **Package Options Include Plastic** A2 L 3 🛛 B2 Small-Outline (DW), Shrink Small-Outline A3 L 4 17 ПВЗ (DB, DBQ), Thin Very Small-Outline (DGV), A4 [5 16 15 B4 and Thin Shrink Small-Outline (PW) A5 🛛 6 14 B5 Packages A6 7 13 B6 A7 [8 description 12 🛛 B7 A8 🛛 9 11 B8 GND 10

NC – No internal connection

The SN74CBT3245A provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When output enable (\overline{OE}) is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3245A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE				
	FUNCTION			
L	A port = B port			
н	Disconnect			

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SCDS002J – NOVEMBER 1992 – REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	115°C/W
	DBQ package	118°C/W
	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T _{stg}		. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	$_{C} = 4.5 \text{ V}, \qquad \qquad I_{I} = -18 \text{ mA}$				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±5	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			50	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
Ci	Control inputs	VI = 3 V or 0				4		pF
C _{io(OFF}	=)	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			4		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V ₁ = 2.4 V,	l _l = 15 mA				
ron¶			$\lambda = 0$	l _l = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	v] = 0	lı = 30 mA		5	7	
			V _I = 2.4 V,	lı = 15 mA		10	15	

[‡] All typical values are at $V_{CC} = 5 V$ (unless otherwise noted), $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC} = 4	v	= ۷ _{CC} ± 0.	= 5 V 5 V	UNIT
			MIN N	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.35		0.25	ns
t _{en}	ŌĒ	A or B		6.4	1.9	5.9	ns
tdis	ŌĒ	A or B		5.7	2.1	6	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SCDS080 - JULY 1998

 Functionally Equivalent to QS3245 Standard '245-Type Pinout 	DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)					
 25-Ω Switch Connection Between Two Ports 	NC $\begin{bmatrix} 1 & 20 \end{bmatrix}$ V _{CC}					
TTL-Compatible Input Levels	A2 3 18 B1					
Package Options Include Plastic	A3 🛛 4 17 🗍 B2					
Small-Outline (DW), Shrink Small-Outline	A4 🛛 5 16 🗍 B3					
(DB, DBQ), Thin Very Small-Outline (DGV),	A5 🚺 6 15 🗍 B4					
and Thin Shrink Small-Outline (PW)	A6 🚺 7 14 🗍 B5					
Packages	A7 🚺 8 13 🗍 B6					
	A8 🚺 9 12 🗍 B7					
description	GND 🛛 10 🛛 11 🗍 B8					

The SN74CBTR3245 provides eight bits of

high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

opagation delay.

NC - No internal connection

The device is organized as one 8-bit switch. When output enable (\overline{OE}) is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The device has equivalent $25 \cdot \Omega$ series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.

The SN74CBTR3245 is characterized for operation from -40°C to 85°C.

FUN					
	FUNCTION				
L	A port = B port				
н	Disconnect				

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	115°C/W
	DBQ package	118°C/W
	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T _{stg}		65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Τ _Α	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITIO	NS	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lı = -18 mA				-1.2	V
lj		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±5	μA
ICC	-	V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			50	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at $V_{\mbox{CC}}$ or GND			3.5	mA
Ci	Control inputs	VI = 3 V or 0						pF
C _{io(OFF}	F)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
			$\lambda = 0$	lj = 64 mA				
r _{on} ¶		$V_{CC} = 4.5 V$	VI = 0	lj = 30 mA				Ω
		l f	$V_{I} = 2.4 V,$	lj = 15 mA				

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} †	A or B	B or A		ns
ten	ŌĒ	A or B		ns
^t dis	ŌĒ	A or B		ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns,
- $t_f \le 2.5$ ns. D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzZ are the same as t_{en} .
- G. tpLH and tpHL are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



D, DB, DBQ, DGV, OR PW PACKAGE (TOP VIEW)

B4

B3 2

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16 🛛 V_{CC}

15 B5

- Functionally Equivalent to QS3251
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3251 is a 1-of-8 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When output enable (\overline{OE}) is low, the SN74CBT3251 is enabled. S0, S1, and S2 select one of the B outputs for the A-input data.

The SN74CBT3251 is characterized for operation from -40°C to 85°C.

(each multiplexer/demultiplexer)						
	INP	EUNCTION				
OE	S2	S 1	S0	FUNCTION		
L	L	L	L	A port = B1 port		
L	L	L	Н	A port = B2 port		
L	L	н	L	A port = B3 port		
L	L	н	Н	A port = B4 port		
L	Н	L	L	A port = B5 port		
L	Н	L	Н	A port = B6 port		
L	Н	Н	L	A port = B7 port		
L	Н	Н	Н	A port = B8 port		
н	Х	Х	Х	Disconnect		

FUNCTION TABLE

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



B2 [3	14] B6
B1 [4	13] B7
A	5	12] B8
NC [6	11] S0
OE [7	10] S1
GND [8	9] S2

NC - No internal connection

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		. –0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I _K (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	113°C/W
	DB package	131°C/W
	DBQ package	139°C/W
	DGV package	180°C/W
	PW package	149°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS MIN TYP [†] MAX UN		UNIT			
VIK		V _{CC} = 4.5 V,	lj = -18 mA			-1.2	V
Ц		$V_{CC} = 5.5 V,$	$V_{I} = 5.5 V \text{ or GND}$			±1	μA
ICC		$V_{CC} = 5.5 V,$	I _O = 0,	$V_{I} = V_{CC}$ or GND		3	μΑ
∆lcc‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		2.5	mA
Ci	Control inputs	V _I = 3 V or 0			3.5		pF
	A port				17.5		۶E
C _{io(OFF)}	B port	$v_{O} = 3 v \text{ or } 0,$	OE = ACC		4		рг
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	l _l = 15 mA	14 20		
r _{on} §			$\lambda = 0$	lj = 64 mA	5	7	Ω
		V _{CC} = 4.5 V	v] = 0	lı = 30 mA	5	7	
			V _I = 2.4 V,	lj = 15 mA	10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO	V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT
		(001101)	MIN MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A	0.35		0.25	ns
^t pd	S	А	6	2	5.5	ns
	S	В	6.4	1.5	5.6	ns
^t en	ŌĒ	A or B	6.4	1.6	5.8	
÷.,	S	В	B 6.8 1.9	6.4		
^ı dis	OE	A or B	6	2.3	6.2	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .





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- Functionally Equivalent to QS3253
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

 $1\overline{OE}$, $2\overline{OE}$, S0, and S1 select the appropriate B output for the A-input data.

The SN74CBT3253 is characterized for operation from -40° C to 85° C.

INPUTS			EUNCTION
OE	S 1	S0	FUNCTION
L	L	L	A port = B1 port
L	L	Н	A port = B2 port
L	Н	L	A port = B3 port
L	Н	Н	A port = B4 port
н	Х	Х	Disconnect

FUNCTION TABLE (each multiplexer/demultiplexer)



D, DB, DBQ, DGV, OR PW PACKAGE (TOP VIEW)						
10E [1	16	V _{CC}			
S1 [2	15	20E			
1B4 [3	14	S0			
1B3 [4	13	2B4			
1B2 [5	12	2B3			
1B1 [6	11	2B2			
1A [7	10	2B1			
GND [8	9	2A			

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		0.5 0.5	V to 7 V V to 7 V
Continuous channel current			128 mA
Input clamp current, I_{K} ($V_{I/O} < 0$)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	1	13°C/W
	DB package	1	31°C/W
	DBQ package	1	39°C/W
	DGV package	1	80°C/W
	PW package	1	49°C/W
Storage temperature range, T _{stg}		–65°C t	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1	μA
ICC		$V_{CC} = 5.5 V,$	I _O = 0,	$V_{I} = V_{CC}$ or GND			3	μΑ
∆lcc [‡]	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				3.5		pF
C	A port	$V_{a} = 2 V_{ar} 0$				10		۶E
Cio(OFF)	B port	$v_{O} = 3 v \text{ or } 0,$	OE = VCC			4		рг
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V ₁ = 2.4 V,	l _l = 15 mA				
r _{on} §			$V_{\rm L} = 0$	l _l = 64 mA		5	7	Ω
-		V _{CC} = 4.5 V	v] = 0	lı = 30 mA		5	7	
			$V_{I} = 2.4 V,$	lj = 15 mA		10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPLIT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
		(001101)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.35		0.25	ns
^t pd	S	A or B		6.6	1.6	6.2	ns
ten	S	A or B		7.1	1.3	6.3	20
	ŌE			7.3	1.4	6.4	ns
^t dis	S	A at D		7.9	1.1	7.4	
	ŌĒ	A or B		7.3	2.3	7	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.





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 Functionally Equivalent to QS3253 25-Q Switch Connection Between Two 	D, DB, DBQ, DGV, OR PW PACKAGE (TOP VIEW)			
Ports				
 TTL-Compatible Input Levels 	S1 [] 2 15 [] 2 0E			
 Package Options Include Plastic 	1B4 🚺 3 14 🗍 S0			
Small-Outline (D), Shrink Small-Outline	1B3 🛛 4 13 🗋 2B4			
(DB, DBQ), Thin Very Small-Outline (DGV),	1B2 🛛 5 12 🗋 2B3			
and Thin Shrink Small-Outline (PW)	1B1 🛛 6 🛛 11 🗍 2B2			
Packages	1A 🛛 7 10 🗍 2B1			
description	GND [8 9] 2A			

The SN74CBTR3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

10E, 20E, S0, and S1 select the appropriate B output for the A-input data.

The device has equivalent $25 \cdot \Omega$ series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.

The SN74CBTR3253 is characterized for operation from -40°C to 85°C.

(ea	(each multiplexer/demultiplexer)							
	INPUTS	EUNCTION						
OE	OE S1 S0		FUNCTION					
L	L	L	A port = B1 port					
L	L	Н	A port = B2 port					
L	Н	L	A port = B3 port					
L	Н	Н	A port = B4 port					
н	Х	х	Disconnect					

FUNCTION TABLE

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N DO
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SCDS081 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		0.5 V to 0.5 V to	7 V 7 V
Continuous channel current		128	mΑ
Input clamp current, I_{K} ($V_{I/O} < 0$)			mΑ
Package thermal impedance, θ_{JA} (see Note 2):	D package	113°C	C/W
	DB package	131°C	C/W
	DBQ package	139°C	C/W
	DGV package	180°C	C/W
	PW package	149°C	C/W
Storage temperature range, T _{sta}		-65°C to 15	0°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS			MIN	түр†	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	lj = -18 mA				-1.2	V
Ц		$V_{CC} = 5 V,$	$V_{I} = 5.5 V \text{ or GND}$				±1	μA
ICC		$V_{CC} = 5.5 V,$	I _O = 0,	$V_{I} = V_{CC}$ or GND			3	μΑ
∆lcc [‡]	Control inputs	$V_{CC} = 5.5 V,$	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_I = 3 V \text{ or } 0$						pF
	A port						۶E	
	B port	vO = 3 v or 0,	OE = VCC					μ
			$V_{\rm L} = 0$	l _l = 64 mA				
ron§	$V_{CC} = 4.5 V$		VI = 0	lı = 30 mA				Ω
			V _I = 2.4 V,	lı = 15 mA				

[†] All typical values are at $V_{CC} = 5 V$ (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT	
tpd¶	A or B	B or A		ns	
^t pd	S	A or B		ns	
	S	A or P			
^l en	ŌĒ			115	
^t dis	S	A or B			
	ŌĒ	AOB		115	

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS081 - JULY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. tpzL and tpzH are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017I - MAY 1995 - REVISED MAY 1998

- Functionally Equivalent to QS3257
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB, DBQ), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3257 is a 4-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Output-enable (\overline{OE}) and select-control (S) inputs select the appropriate B1 and B2 outputs for the A-input data.

The SN74CBT3257 is characterized for operation from -40° C to 85° C.

D, DB, DBQ, OR PW PACKAGE (TOP VIEW)						
	\mathbf{U}^{-}					
1	16	l [∨] cc				
2	15] oe				
3	14] 4B1				
4	13] 4B2				
5	12] 4A				
6	11] 3B1				
7	10] 3B2				
8	9] 3A				
	Q , (TO 1 2 3 4 5 6 7 8	Q , OR PW TOP VIEW 1 16 2 15 3 14 4 13 5 12 6 11 7 10 8 9				

INPU	JTS	EUNCTION
OE	S	FUNCTION
L	L	A port = B1 port
L	Н	A port = B2 port
н	Х	Disconnect



SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017I - MAY 1995 - REVISED MAY 1998

logic diagram (positive logic)




SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017I - MAY 1995 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5 V to 7 V -0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, $I_K (V_{I/O} < 0)$		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	113°C/W
	DB package	131°C/W
	DBQ package	139°C/W
	PW package	149°C/W
Storage temperature range, T _{stg}		65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS		MIN	түр‡	MAX	UNIT			
VIK		$V_{CC} = 4.5 V,$	lı = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		$V_{CC} = 5.5 V,$	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			3	μA
∆ICC§	Control inputs	$V_{CC} = 5.5 V,$	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0				3.5		pF
	A port	$V_{0} = 3 V_{0} r 0$	$\overline{OE} = V_{CC}$			6.5		ъЕ
	B port	vO = 3 v or 0,				4		рг
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		14	20	
ron¶			$\lambda = 0$	lı = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	vi - 0	lj = 30 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017I - MAY 1995 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT	
		(001101)	MIN MAX	MIN	MAX		
t _{pd} †	A or B	B or A	0.35		0.25	ns	
^t pd	S	А	5.5	1.6	5	ns	
ten	S	В	5.7	1.6	5.2	ns	
	OE	A or B	5.6	1.8	5.1		
^t dis	S	В	5.2	1	5	200	
	ŌĒ	A or B	5.5	2.2	5.5	115	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.





SN74CBT3306 DUAL FET BUS SWITCH

SCDS016E - MAY 1995 - REVISED MAY 1998

D OR PW PACKAGE (TOP VIEW)

8 Vcc

7

5

12OE

6 🛛 2B

1 2A

1 OE

GND [

1A [

1B [3

2

4

- **5-** Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is high.

The SN74CBT3306 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE (each bus switch)

	FUNCTION
L	A port = B port
н	Disconnect

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN74CBT3306 DUAL FET BUS SWITCH

SCDS016E - MAY 1995 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I_{K} ($V_{I/O} < 0$)	
Package thermal impedance, θ_{JA} (see Note 2): [D package 197°C/W
F	PW package 243°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS		MIN	түр‡	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆lCC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				3		pF
Cio(OFF)		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			4		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V ₁ = 2.4 V,	l _l = 15 mA		14	20	
r _{on} ¶			N/ 0	l _l = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	v] = 0	l _l = 30 mA		5	7	
			$V_{I} = 2.4 V,$	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

\$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBT3306 DUAL FET BUS SWITCH

SCDS016E - MAY 1995 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.35		0.25	ns
ten	ŌĒ	A or B		5.6	1.8	5	ns
tdis	OE	A or B		4.6	1	4.3	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns. t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SCDS027D - MAY 1995 - REVISED MAY 1998

- Standard '245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3345 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

(TOP VIEW)						
oe [1	Ο	20]v _{cc}		
A1 [2		19] OE		
A2 🛛	3		18] B1		
АЗ 🛛	4		17	B2		
A4 [5		16] B3		
A5 🛛	6		15] B4		
A6 [7		14] B5		
A7 [8		13] B6		
A8 [9		12] B7		
GND [10		11] B8		

DB, DGV, DW, OR PW PACKAGE

The device is organized as one 8-bit switch bank with dual output-enable (OE and \overline{OE}) inputs. When \overline{OE} is low or OE is high, the switch is on and port A is connected to port B. When \overline{OE} is high and OE is low, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3345 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE				
	FUNCTION			
L	A port = B port			
н	Disconnect			

logic diagram (positive logic)





SCDS027D - MAY 1995 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		-0.5 V to 7 V -0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	115°C
	DGV package	146°C
	DW package	97°C
	PW package	128°C
Storage temperature range, T _{stg}	······································	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТА	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			түр‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
li		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	l _O = 0,	$V_{I} = V_{CC}$ or GND			50	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
Ci	Control inputs	V _I = 3 V or 0				3		pF
Cio(OFF)		V _O = 3 V or 0,	$\overline{OE} = V_{CC} \text{ or } OE = GI$	ND		6		pF
ron¶			$\lambda = 0$	lı = 64 mA		5	7	
		V _{CC} = 4.5 V	V] = 0	lı = 30 mA		5	7	Ω
			V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V, $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SCDS027D - MAY 1995 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER			= V _{CC} ± 0.	UNIT	
		(001-01)	MIN	MAX	
t _{pd} †	A or B	B or A		0.25	ns
t _{en}	OE or OE	A or B	1	9.1	ns
^t dis	OE or OE	A or B	1	8.7	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. t_{PZI} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS003I - NOVEMBER 1992 - REVISED MAY 1998

- Functionally Equivalent to QS3383 and QS3L383
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB, DBQ), and Thin Shrink Small-Outline (PW) Packages, Ceramic DIPs (JT), and Ceramic Flat (W) Package

description

The 'CBT3383 devices provide ten bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The devices operate as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when BE is low.

The SN54CBT3383 is charaterized for operation over the full military temperature range of –55°C to 125°C. The SN74CBT3383 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE							
INP	UTS	INPUTS/OUTPUTS					
BE	ВΧ	1A1–5A1	1A2–5A2				
L	L	1B1–5B1	1B2–5B2				
L	Н	1B2–5B2	1B1–5B1				
н	Х	Z	Z				

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN74CBT3383 DB, DBQ, DW, OR PW PACKAGE (TOP VIEW)							
BE [1B1 [1A1 [1A2 [1B2 [2B1 [2A2 [2B2 [3B1 [3A1 [3A1 [1 2 3 4 5 5 6 7 7 8 9 10 11	24 V _{CC} 23 5B2 22 5A2 21 5A1 20 5B1 19 4B2 18 4A2 17 4A1 16 4B1 15 3B2 14 3A2					
<u> </u>							

SN54CBT3383 . . . JT OR W PACKAGE

SCDS003I - NOVEMBER 1992 - REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range Voo		-0.5 V to 7 V
		. 0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DBQ package	113°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}	· · · · · · · · · · · · · · · · · · ·	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



SCDS003I - NOVEMBER 1992 - REVISED MAY 1998

recommended operating conditions (see Note 3)

		SN54CBT3383		SN74CB		
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level control input voltage	2		2		V
VIL	Low-level control input voltage		0.8		0.8	V
TA	Operating free-air temperature	-55	125	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54CBT3383		SN74CBT3383		83			
		1	TEST CONDITIONS		MIN	түр†	MAX	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2			-1.2	V
Ц		V _{CC} = 5.5 V,	VI = 5.5 V or	GND			±5			±1	μΑ
ICC	_	$V_{CC} = 5.5 V,$	l _O = 0,	$V_I = V_{CC}$ or GND			50			50	μΑ
∆ICC [‡]	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					2.5			2.5	mA
C.	Control inputo	V _I = 3 V or 0						3		۶E	
	Control inputs	V _I = 2.5 V	V _I = 2.5 V				5				рг
		$V_{O} = 3 V \text{ or } 0,$	$\overline{BE} = V_{CC}$						6		ņΕ
└io(OFF)		V _O = 2.5 V,	$\overline{BE} = V_{CC}$				6				μ
			$\lambda = 0$	lı = 64 mA		5	9.2		5	7	
r _{on} §	$V_{CC} = 4.5 V$	vj=0	lı = 30 mA					5	7	Ω	
			V _I = 2.4 V,	l _l = 15 mA		10	17		10	15	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	SN54CE	BT3383	SN74CB	T3383	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UNIT
t _{pd} ¶	A or B	B or A		1.5		0.25	ns
^t pd	BX	A or B	1	10.2	1	9.2	ns
ten	BE	A or B	1	10.8	1	8.6	ns
t _{dis}	BE	A or B	1	8.2	1	7.5	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS003I - NOVEMBER 1992 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.





SN74CBTH3383 10-BIT FET BUS-EXCHANGE SWITCH WITH BUS HOLD

SCDS023G - MAY 1995 - REVISED OCTOBER 1998

 Functionally Equivalent to QS3388 5-Ω Switch Connection Between Two Ports 	DB, DW, OR PW PACKAGE (TOP VIEW)
TTL-Compatible Input Levels	
 Bus Hold on Data Inputs/Outputs	1B1 2 23 5B2
Eliminates the Need for External	1A1 3 22 5A2
Pullup/Pulldown Resistors	1A2 4 21 5A1
 Package Options Include Plastic	1B2 5 20 5B1
Small-Outline (DW), Shrink Small-Outline	2B1 6 19 4B2
(DB), and Thin Shrink Small-Outline (PW)	2A1 7 18 4A2
Packages	2A2 8 17 4A1
description	3B1 [10 15] 3B2
The SN74CBTH3383 provides ten bits of	3A1 [11 14] 3A2
bich speed TTL compatible bus switching or	GND [12 13] BX

high-speed TTL-compatible bus switching or exchanging with bus hold on all I/Os. The low on-state resistance of the switch allows connection to be made with minimal propagation delay.

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when \overline{BE} is low. The switches are open when \overline{BE} is high. Active bus-hold circuitry is provided to hold unused or floating data inputs/outputs at a valid logic level.

When the switch is turned off, the bus-hold circuit pulls all I/Os to V_{CC} or to GND, depending on the last-known state of the pin. The bus-hold feature is active only when the SN74CBTH3383 I/Os are in the high-impedance state.

The SN74CBTH3383 is characterized for operation from -40°C to 85°C.

	FUNCTION TABLE								
INP	UTS	INPUTS/0	OUTPUTS	FUNCTION					
BE	ВΧ	A1 PORT	A2 PORT	FUNCTION					
L	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port					
L	Н	B2 port	B1 port	A2 port = B2 port A2 port = B1 port					
н	х	Z	Z	Disconnect All ports = bus hold					



SN74CBTH3383 10-BIT FET BUS-EXCHANGE SWITCH WITH BUS HOLD

SCDS023G - MAY 1995 - REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} to V _{DD}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



SN74CBTH3383 **10-BIT FET BUS-EXCHANGE SWITCH** WITH BUS HOL

SCDS023G - MAY 1995 - REVISED OCTOBER 1998

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITION	ONS	MIN	түр†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lı = –18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1	μΑ
I _{BHL} ‡		V _{CC} = 4.5 V,	V _I = 0.8 V		100			μΑ
I _{BHH} §		V _{CC} = 4.5 V,	V _I = 2 V		-100			μΑ
IBHLO		V _{CC} = 5.5 V,	$V_{I} = 0$ to 5.5 V		500			μA
Івнно [‡]	ŧ	V _{CC} = 5.5 V,	$V_{I} = 0$ to 5.5 V		-500			μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μΑ
∆ICC	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				3		pF
C _{io(OFF}	=)	V _O = 3 V or 0,	$\overline{BE} = V_{CC}$			6		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4,	lj = 15 mA		16	22	
ron☆			$V_{i} = 0$	l _l = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	vI=0	lı = 30 mA		5	7	
			$V_{I} = 2.4 V,$	I _I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡]The bus hold circuit can sink at least the minimum low sustaining current at VIL max. IBHL should be measured after lowering VIN to GND and then raising it to VIL max.

§ The bus hold circuit can source at least the minimum high sustaining current at VIH min. IBHH should be measured after raising VIN to VCC and then lowering it to VIH min.

 \P An external driver must source at least IBHLO to switch this node from low to high.

An external driver must sink at least IBHHO to switch this node from high to low.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

*Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		TO $V_{CC} = 4 V \frac{V_C}{\pm}$		= ۷ _{CC} ± 0.	V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	
t _{pd} □	A or B	B or A		0.35		0.25	ns
^t pd	BX	A or B		10.2	1	9.2	ns
t _{en}	BE	A or B		9.6	1	8.6	ns
^t dis	BE	A or B		8.5	1	7.5	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

SCDS023G - MAY 1995 - REVISED OCTOBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns. t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. tPLH and tPHL are the same as tpd.





SCDS082 - JULY 1998

 Functionally Equivalent to QS3383 and QS3L383 	DB, DBQ, DW, OR PW PACKAGE (TOP VIEW)
 25-Ω Switch Connection Between Two Ports 	BE 1 24 V _{CC} 1B1 2 23 5B2
TTL-Compatible Input Levels	1A1 🛛 3 22 🗍 5A2
Package Options Include Plastic	1A2 🛛 4 21 🗋 5A1
Small-Outline (DW), Shrink Small-Outline	1B2 🛛 5 20 🗍 5B1
(DB, DBQ), and Thin Shrink Small-Outline	2B1 🛛 6 19 🗍 4B2
(PW) Packages	2A1 🚺 7 18 🗍 4A2
(). aonagoo	2A2 🛛 8 17 🗍 4A1
description	2B2 🛛 9 16 🗍 4B1
	3B1 🚺 10 15 🗍 3B2
The SN74CBTR3383 device provides ten bits of	3A1 🚺 11 14 🗍 3A2
high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the	GND [12 13] BX

high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high. The switch is connected when \overline{BE} is low.

The device has equivalent $25 \cdot \Omega$ series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.

The SN74CBTR3383 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE						
INP	UTS	INPUTS/0	OUTPUTS			
BE	ΒХ	1A1–5A1	1A2–5A2			
L	L	1B1–5B1	1B2–5B2			
L	Н	1B2–5B2	1B1–5B1			
н	Х	Z	Z			



SCDS082 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		-0.5 V to 7 V -0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DBQ package	113°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}	·····	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51.



SCDS082 - JULY 1998

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC	-	V _{CC} = 5.5 V,	I _O = 0,	$V_{I} = V_{CC}$ or GND			50	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at $V_{\mbox{CC}}$ or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0						pF
C _{io(OFF}	=)	$V_{O} = 3 V \text{ or } 0,$	$\overline{BE} = V_{CC}$					pF
			$V_{1} = 0$	lı = 64 mA				
r _{on} §		$V_{CC} = 4.5 V$	VI = 0	l _l = 30 mA				Ω
			$V_{I} = 2.4 V,$	lj = 15 mA				

[†] All typical values are at V_{CC} = 5 V, $T_A = 25^{\circ}C$.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} ¶	A or B	B or A		ns
^t pd	BX	A or B		ns
t _{en}	BE	A or B		ns
tdis	BE	A or B		ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS082 - JULY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. tpLZ and tpHZ are the same as tdis.

F. t_{PZL} and t_{PZH} are the same as t_{en}. G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS004I - NOVEMBER 1992 - REVISED MAY 1998

 Functionally Equivalent to QS3384 and QS3L384 	DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)
 5-Ω Switch Connection Between Two Ports 	
TTL-Compatible Input Levels	1B1 2 23 2B5
 Package Options Include Plastic 	1A1 🛛 3 22 🗍 2A5
Small-Outline (DW), Shrink Small-Outline	1A2 🛛 4 🛛 21 🗍 2A4
(DB, DBQ), Thin Very Small-Outline (DGV),	1B2 🛛 5 🛛 20 🗍 2B4
and Thin Shrink Small-Outline (PW)	1B3 🛛 6 🛛 19 🗍 2B3
Packages	1A3 🛛 7 🛛 18 🗍 2A3
	1A4 🛛 8 🛛 17 🗍 2A2
description	1B4 🛛 9 16 🗍 2B2
The SN74CBT2284A provides top hits of	1B5 🛛 10 🛛 15 🗍 2B1
high speed TTL compatible bus switching. The	1A5 🛛 11 🛛 14 🗍 2A1
low on-state resistance of the switch allows	GND [] 12 13 [] 2 0E
connections to be made with minimal propagation	

The device is organized as two 5-bit switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3384A is characterized for operation from -40°C to 85°C.

(each 5-bit bus switch)					
INPUTS INPUTS/OUTPUTS					
1 <mark>0E</mark>	2 <mark>0E</mark>	1B1–1B5	2B1–2B5		
L	L	1A1–1A5	2A1–2A5		
L	Н	1A1–1A5	Z		
н	L	Z	2A1–2A5		
н	Н	Z	Z		

FUNCTION TABLE

logic diagram (positive logic)

delay.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DBQ package	113°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITIONS			TYP‡	MAX	UNIT
VIК		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0				4		pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			4.5		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	l _l = 15 mA		14	20	
r _{on} ¶			$V_{i} = 0$	l _l = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	VI = 0	lı = 30 mA		5	7	
			V _I = 2.4 V,	l _l = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

If Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



SCDS004I - NOVEMBER 1992 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.35		0.25	ns
ten	ŌĒ	A or B		6.2	1.9	5.7	ns
t _{dis}	ŌĒ	A or B		5.5	2.1	5.2	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns. D. The outputs are measured one at a time with one transition per measurement.
- D. The outputs are measured one at a time with one
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SCDS083 - JULY 1998

 Functionally Equivalent to QS3384 and QS3L384 	DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)
 25-Ω Switch Connection Between Two Ports 	1 0E 1 24 V _{CC} 1B1 2 23 285
TTL-Compatible Input Levels	1A1 🚺 3 22 🗍 2A5
 Package Options Include Plastic 	1A2 🚺 4 21 🗍 2A4
Small-Outline (DW), Shrink Small-Outline	1B2 🛛 5 20 🗍 2B4
(DB, DBQ), Thin Very Small-Outline (DGV),	1B3 🛛 6 🛛 19 🗍 2B3
and Thin Shrink Small-Outline (PW)	1A3 🚺 7 🛛 18 🗍 2A3
Packages	1A4 🚺 8 17 🗍 2A2
	1B4 🛛 9 16 🗍 2B2
description	1B5 🚺 10 15 🗍 2B1
The SN7/CBTR338/ provides ten hits of	1A5 🚺 11 🛛 14 🗋 2A1
high-speed TTL-compatible bus switching. The	GND [12 13] 20E

high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The device has equivalent $25 \cdot \Omega$ series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.

The SN74CBTR3384 is characterized for operation from -40°C to 85°C.

(each 5-bit bus switch)						
INP	UTS	INPUTS/OUTPUTS				
10E	2 <mark>0E</mark>	1B1–1B5	2B1–2B5			
L	L	1A1–1A5	2A1–2A5			
L	Н	1A1–1A5	Z			
н	L	Z	2A1–2A5			
н	н	Z	Z			

FUNCTION TABLE

PRODUCT PREVIEW



SCDS083 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DBQ package	113°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		S5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _C C	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCDS083 - JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_{I} = 5.5 \text{ V or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	lO = 0,	$V_I = V_{CC}$ or GND			3	μA
∆lCC [‡]	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0						pF
Cio(OFF)		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
			$\lambda t = 0$	lj = 64 mA				
r _{on} §		$V_{CC} = 4.5 V$	V = 0	lı = 30 mA				Ω
			V _I = 2.4 V,	lj = 15 mA				

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} ¶	A or B	B or A		ns
ten	ŌĒ	A or B		ns
^t dis	ŌĒ	A or B		ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. tpLZ and tpHZ are the same as tdis.

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. tPLH and tPHL are the same as tpd.



SCDS022F - MAY 1995 - REVISED MAY 1998

- **Functionally Equivalent to QS3386**
- 5- Ω Switch Connection Between Two Ports
- **TTL-Compatible Input Levels**
- Uses V_{CC} of 5 V and V_{DD} of -2 V
- **Package Options Include Plastic Shrink** Small-Outline (DB), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3386 provides ten bits of high-speed TTL-compatible bus switching or exchanging. The input signals can range from -2 V to 5 V. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

DB, DW, OR PW PACKAGE (TOP VIEW)					
BE [1B1 [1A1 [1A2 [2B1 [2A1 [2A2 [2B2 [3B1 [3A1 [V _{DD} [1 2 3 4 5 6 7 8 9 10 11 12	24 23 22 21 20 19 18 17 16 15 14 13	Vcc 582 542 541 581 482 442 441 481 382 342 342 8X		

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which allows swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high. The switches are disconnected when BE is high.

The SN74CBT3386 is characterized for operation from -40°C to 85°C.

T UNCTION TABLE						
INP	UTS	INPUTS/OUTPUTS				
BE	BX	1A1–5A1	1A2–5A2			
L	L	1B1–5B1	1B2–5B2			
L	н	1B2–5B2	1B1–5B1			
н	Х	Z	Z			

EUNCTION TABLE

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



SCDS022F - MAY 1995 - REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} to V _{DD} Supply voltage range, V _{DD}		
Input voltage range, V _I (see Note 1)		$V_{DD} - 0.5$ V to V_{DD} + 7.5 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



SCDS022F - MAY 1995 - REVISED MAY 1998

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	ΤΥΡ [†] ΜΑΧ	UNIT				
VIK		V _{CC} = 4.5 V,	lj = -18 mA			V _{DD} -1.2	V				
Ц		V _{CC} = 5.5 V,	V _I = 5.5 V or GND		V _I = 5.5 V or GND		V _I = 5.5 V or GND			±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_{I} = V_{CC}$ or GND		3	μΑ				
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		5	mA				
Ci	Control inputs	V _I = 3 V or 0					pF				
C _{io(OFF}	-)	$V_{O} = 3 V \text{ or } 0,$	$\overline{BE} = V_{CC}$				pF				
		$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4,	lj = 15 mA							
r _{on} §			$V_{i} = 0$	lı = 64 mA			Ω				
UII		$V_{CC} = 4.5 V$	VI = 0	lı = 30 mA							
			V _I = 2.4 V,	lj = 15 mA							

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two terminals.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		FROM TO (INPUT) (OUTPUT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V	
		(001201)	MIN	MAX	MIN	MAX	
tpd¶	A or B	B or A					ns
	BX	A or P					20
^l en	BE						115
tdis	BE	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS022F - MAY 1995 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. tPLH and tPHL are the same as tpd.





- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Shrink Small-Outline (DL) and Small-Outline (DW) Packages

description

The SN74CBT3390 is an 8-bit to 16-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, in which two different banks of memory must be addressed simultaneously. This also can be used to connect or isolate the PCI bus to one or two slots simultaneously.

Two output enables ($\overline{OE1}$ and $\overline{OE2}$) control the data flow. When $\overline{OE1}$ is low, A port is connected to 1B port. When $\overline{OE2}$ is low, A port is connected to 2B port. When both $\overline{OE1}$ and $\overline{OE2}$ are low, the A port is connected to both 1B and 2B ports. The control inputs can be driven with a 5-V CMOS, 5-V TTL, or an LVTTL driver.

The SN74CBT3390 is characterized for operation from -40° C to 85° C.

FUNC	TION	TABLE	

INP	UTS	EUNCTION
OE1	OE2	FUNCTION
L	L	A = 1B and $A = 2B$
L	н	A = 1B
н	L	A = 2B
н	н	Isolation

DL O	r dv (top	V PACH VIEW)	(AGE
1B1 [2B1 [A1 [1 2 3	28 27 26	V _{CC} 1B8 2B8
1B2 [2B2 [4 5	25 24	A8
A2	6	23	2B7
1B3 [2B3 [7 8	22 21	A7 1B6
A3 [9	20	2B6
1B4 L 2B4 [10 11	19 18	D A6] 1B5
	12	17 16	2B5
GND [14	15	

SCDS071 - JULY 1998



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DL package	97°C/W
DW package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
		$V_{CC} = 0$	VI = 5.5 V				10	
1		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	IO = 0,	$V_I = V_{CC} \text{ or } GND$			3	μA
∆lcc‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other input at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$						pF
C _{io(OFF})	$V_{O} = 3 V \text{ or } 0$						pF
			$\lambda = 0$	l _l = 64 mA				
r _{on} §		V _{CC} = 4.5 V	V] = 0	l _l = 30 mA				Ω
			$V_1 = 2.4 V_2$	lı = 15 mA				

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A			ns
^t en	ŌĒ	A or B			ns
^t dis	ŌĒ	A or B			ns

The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.





SCDS061B - APRIL 1998 - REVISED AUGUST 1998

- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DBQ), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT3861 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit switch with a single output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

The SN74CBT3861 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE

	FUNCTION
L	A port = B port
Н	Disconnect

logic diagram (positive logic)





DBQ, DW, OR PW PACKAGE (TOP VIEW)			
NC [A1 [A2 [A3 [A5 [A5 [A7 [A8 [A9 [A10]	1 2 3 4 5 6 7 8 9 10 11	24 23 22 21 20 19 18 17 16 15 14	V _{CC} 0E B1 B2 B3 B4 B5 B6 B7 B8 B9
GND	12	13	

NC – No internal connection
SN74CBT3861 10-BIT FET BUS SWITCH

SCDS061B - APRIL 1998 - REVISED AUGUST 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range V		
Supply voltage range, v _{CC}		$0.5 \times 107 \times 107$
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	113°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		$-65^{\circ}C$ to $150^{\circ}C$

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТА	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_{I} = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0				3		pF
Cio(OFF)		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			5		pF
ron¶		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lı = 15 mA		14	22	
			$V_{i} = 0$	lı = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	VI = 0	lı = 30 mA		5	7	
		$V_{I} = 2.4 V,$	V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



SN74CBT3861 **10-BIT FET BUS SWITCH**

SCDS061B - APRIL 1998 - REVISED AUGUST 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT	
		(001101)	MIN	MAX	MIN	MAX		
t _{pd} †	A or B	B or A		0.35		0.25	ns	
ten	ŌĒ	A or B		8.1	3.8	7.5	ns	
t _{dis}	ŌĒ	A or B		6.3	3.4	6.6	ns	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBT6800 10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS FOR LIVE INSERTION SCDS005I – MARCH 1993 – REVISED MAY 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT6800 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

DB, DW, OR PW PACKAGE						
	(
ON	1	U	24] v _{cc}		
A1	2		23] B1		
A2	3		22] B2		
A3	4		21] B3		
A4	5		20] B4		
A5	6		19] B5		
A6	7		18] B6		
A7	8		17] B7		
A8	9		16] B8		
A9	10		15	B9		
A10	11		14	B10		
GND	12		13	BIASV		

The SN74CBT6800 is organized as one 10-bit switch with a single enable (\overline{ON}) input. When \overline{ON} is low, the switch is on and port A is connected to port B. When \overline{ON} is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10-k Ω resistor.

The SN74CBT6800 is characterized for operation from –40°C to 85°C.

	FUNCTION TABLE						
ON	B1–B10	FUNCTION					
L	A1–A10	Connect					
Н	BIASV	Precharge					

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN74CBT6800 10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS FOR LIVE INSERTION

SCDS005I – MARCH 1993 – REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5 V to 7 V
Blas voltage range, BIASV		0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	VCC	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	түр‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±5	μA
IO		V _{CC} = 4.5 V,	BIASV = 2.4 V,	V _O = 0	0.25			mA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			50	μA
∆ICC§	Control inputs	V _{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				3.5		pF
C _{O(OFF)}		V _O = 3 V or 0,	Switch off			4.5		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V ₁ = 2.4 V,	lj = 15 mA		14	20	
r _{on} ¶			V/- 0	lj = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	vI=0	lı = 30 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBT6800 **10-BIT FET BUS SWITCH** WITH PRECHARGED OUTPUTS FOR LIVE INSERT SCDS005I - MARCH 1993 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPLIT)	FROM TO		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			(001101)	MIN MA	Х	MIN	MAX		
tpd [†]		A or B	B or A	0.3	35		0.25	ns	
^t PZH	BIASV = GND	ŌN	A or P	ç	.1	3.1	8.1	20	
^t PZL	BIASV = 3 V			ç	.6	3.6	8.6	115	
^t PHZ	BIASV = GND		A or P	5	.9	2.7	6.1	20	
^t PLZ	BIASV = 3 V		AUB	6	.4	3	7.3	115	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



- - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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SN54CBT16209 . . . WD PACKAGE

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- **5**-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), 300-mil Shrink Small-Outline (DL), and 380-mil Fine-Pitch Ceramic Flat (WD) Packages

description

The SN54CBT16209 and SN74CBT16209A devices provide 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switches allows connections to be made with minimal propagation delay.

The devices operate as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

The SN54CBT16209 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74CBT16209A is characterized for operation from -40° C to 85° C.

SN74CBT16209A	. DGG, (TOP VI	DGV, OR DL PACKAGE EW)
L		,
S0 [1	48 S1
1A1 [2	47 S2
1A2 [3	46 1 1B1
GND [4	45 3 1B2
2A1 [5	44 2 B1
2A2 [6	43 2B2
V _{CC} [7	42 GND
3A1 [8	41 3B1
3A2 [9	40 3B2
GND [10	39 🛛 GND
4A1 [11	38 4B1
4A2 [12	37 🛛 4B2
5A1 [13	36 5 B1
5A2 [14	35 5 B2
GND [15	34 🛛 GND
6A1 [16	33 6B1
6A2 [17	32 6B2
7A1 [18	31 7B1
7A2 [19	30 7B2
GND [20	29 GND
8A1 [21	28 8B1
8A2 [22	27 🛛 8B2
9A1 [23	26 🛛 9B1
9A2 [24	25 🛛 9B2

			FUNCTIO	NIADLE	
	INPUTS			OUTPUTS	FUNCTION
S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	Н	B1	Z	A1 port = B1 port
L	н	L	B2	Z	A1 port = B2 port
L	н	Н	Z	B1	A2 port = B1 port
н	L	L	Z	B2	A2 port = B2 port
н	L	н	Z	Z	Disconnect
н	Н	L	B1	B2	A1 port = B1 port A2 port = B2 port
н	н	н	B2	B1	A1 port = B2 port A2 port = B1 port

FUNCTION TABLE

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1998, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SCDS006K - NOVEMBER 1992 - REVISED MAY 1998

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I_{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{sta}		–65°C te	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54CBT16209 SN74CBT16209A				
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	4	5.5	V
VIH	High-level control input voltage	2		2		V
VIL	Low-level control input voltage		0.8		0.8	V
Т _А	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITION	ONS	MIN	түр‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
		$V_{CC} = 0,$	V _I = 5.5 V				10	ıιΔ
1		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1	μΛ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				4		pF
C _{io(OFF)}		$V_{O} = 3 V \text{ or } 0,$	S0, S1, or S2 = V _{CC}	;		7.5		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lı = 15 mA				
ron¶			$V_{1} = 0$	lı = 64 mA		4	8	Ω
		V _{CC} = 4.5 V	VI-0	lı = 30 mA		4	8	
			V _I = 2.4 V,	lj = 15 mA		6	15	

[‡] All typical values are at $V_{CC} = 5 V$ (unless otherwise noted), $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

				SN54CE	ST16209		S	N74CB	T16209A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} :	= 4 V	: V _{CC} ± 0	= 5 V 5 V	V _{CC} =	= 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tpd [†]	A or B	B or A				0.8*		0.35		0.25	ns
^t pd	S	A or B		14	2	13.1		9.9	1.5	9	ns
t _{en}	S	A or B		16	1.7	15.3		10.3	1.5	9.8	ns
tdis	S	A or B		14.5	1	13.2		9.3	1.5	8.8	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \le 10 MHz, Z_Q = 50 Ω , t_f \le 2.5 ns, t_f \le 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tPLH and tPHL are the same as tpd.





SCDS033C - APRIL 1997 - REVISED MAY 1998

- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

The SN74CBT16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as a dual 10-bit bus switch with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the ports.

The SN74CBT16210 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 10-bit bus switch)

	FUNCTION
L	A port = B port
Н	Disconnect

logic diagram (positive logic)

1Δ1	2	46	1B1
• • 1A10	12	36	• • 1B10
1 <mark>0E</mark>			
244	13	35	204
2A1 ·	24	25	2B1 • • 2B10
20E	47		



		J 40							
		48							
1A1 [2	47							
1A2 [3	46	1B1						
1A3 [4	45]1B2						
1A4 [5	44] 1B3						
1A5 [6	43]1B4						
1A6 [7	42] 1B5						
GND [8	41	GND						
1A7 [9	40	1B6						
1A8 [10	39] 1B7						
1A9 [11	38	1B8						
1A10	12	37]1B9						
2A1 [13	36	1 B10						
2A2 [14	35	2B1						
v _{cc} [15	34	2B2						
2A3 [16	33	2B3						
GND [17	32	GND						
2A4 [18	31	2B4						
2A5 [19	30	2B5						
2A6 [20	29	2B6						
2A7 [21	28	2B7						
2A8 [22	27	2B8						
2A9 [23	26	2B9						
2A10 [24	25	2B10						

DGG, DGV, OR DL PACKAGE

NC - No internal connection

SCDS033C - APRIL 1997 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I_{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{sta}	· -	–65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТĄ	Operating free-air temperature	-40	85	°C
-				

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
1.		$V_{CC} = 0 V,$	V _I = 5.5 V				10	
1		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				4.5		pF
Cio(OFF)		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			5.5		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		14	20	
ron¶			$V_{i} = 0$	lı = 64 mA		5	7	Ω
-		V _{CC} = 4.5 V	v] = 0	lı = 30 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		8	12	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

 \S This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



SCDS033C - APRIL 1997 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC} = 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
	(INFOT)		MIN MAX	MIN	MAX	
t _{pd} †	A or B	B or A	0.35		0.25	ns
ten	ŌĒ	A or B	9.3	3.3	8.6	ns
tdis	ŌE	A or B	7.1	2.8	7.9	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tPLZ and tPHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS072 - JULY 1998

 25-Ω Switch Connection Between Two Ports 	DGG, DGV, OR DL PACKAGE (TOP VIEW)
 TTL-Compatible Input Levels Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages 	NC 1 48 1 <u>OE</u> 1A1 2 47 2 <u>OE</u> 1A2 3 46 1B1 1A3 4 45 1B2
	1A4 [] 5 44 [] 1B3 1A5 [] 6 43 [] 1B4
description	1A6 🛛 7 42 🗍 1B5
The SN74CBTR16210 provides 20 bits of	GND 8 41 GND
high-speed TTL-compatible bus switching. The	1A7 🚺 9 40 🗍 1B6
low on-state resistance of the switch allows	1A8 🚺 10 🛛 39 🗍 1B7
connections to be made with minimal propagation	1A9 🛛 11 🛛 38 🗍 1B8
delay.	1A10 🛛 12 🛛 37 🗍 1B9
The device is organized as a dual 10-bit bus	2A1 🛛 13 🛛 36 🗋 1B10
switch with separate output-enable (\overline{OF}) inputs. It	2A2 🛛 14 🛛 35 🖸 2B1
can be used as two 10-bit bus switches or as one	V _{CC} [] 15 34 [] 2B2
20-bit bus switch. When \overline{OE} is low, the associated	2A3 🛛 16 🛛 33 🗋 2B3
10-bit bus switch is on and port A is connected to	
port B. When \overline{OE} is high, the switch is open, and	2A4 🛛 ¹⁸ ³¹ 🖉 2B4
a high-impedance state exists between the ports.	2A5 4 ¹⁹ ³⁰ 2B5
	2A6 2^{20} 29 2^{29} 286
I ne device has equivalent 25-12 series resistors to	2A7 4^{21} 28 4^{28}
neduce signal-reflection moise. This eliminates the	^{2A8} 2^{22} 2^{7} 2^{288}
הבכט זטו פאנפוזומו נפוזוווזמנוווץ ופטוטנטוט.	^{2A9} H^{23} ²⁶ H^{2B9}
The SN74CBTR16210 is characterized for	2A10 🛛 ²⁴ 25 🗳 2B10

The SN74CBTR16210 is characterized for operation from -40° C to 85° C.

2710 6	- ·		12010
NC – No	o interr	nal con	nection

FUNCTION TABLE (each 10-bit bus switch)

	FUNCTION
L	A port = B port
н	Disconnect



SCDS072 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	V to 7 V
Input voltage range, V _I (see Note 1)		-0.5	V to 7 V $$
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2)	: DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{sto}		65°C f	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITION	ONS	MIN	түр†	MAX	UNIT
۷IK		$V_{CC} = 4.5 V,$	l _l = –18 mA				-1.2	V
		$V_{CC} = 0 V,$	VI = 5.5 V				10	
'I		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
$\Delta I C C^{\ddagger}$	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$						pF
C _{io(OFF)})	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
			$V_{\rm t} = 0$	l _l = 64 mA				
r _{on} §		V _{CC} = 4.5 V	V] = 0	lı = 30 mA				Ω
			$V_{I} = 2.4 V_{,}$	l _l = 15 mA				

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A			ns
^t en	ŌĒ	A or B			ns
^t dis	ŌĒ	A or B			ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. tpLH and tpHL are the same as t_{pd} .





SCDS028H - JULY 1995 - REVISED MAY 1998

- **5-** Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

The SN74CBT16211A provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a dual 12-bit bus switch or single 24-bit bus switch. When $1\overline{OE}$ is low, 1A is connected to 1B. When $2\overline{OE}$ is low, 2A is connected to 2B.

The SN74CBT16211A is characterized for operation from -40° C to 85°C.

FUNCTION TABLE (each 12-bit bus switch)

INPUTS		INPUTS/0	OUTPUTS		
10E	2 <mark>0E</mark>	1A, 1B 2A, 2B			
L	L	1A = 1B	2A = 2B		
L	Н	1A = 1B	Z		
н	L	Z	2A = 2B		
н	Н	Z	Z		

DGG, DGV, OR DL PACKAGE (TOP VIEW)				
DGG, DG NC [1A1] 1A2 [1A3] 1A4] 1A5 [1A6] 1A7 [1A8] 1A10 [1A11] 1A10] 1A10 [1A11] 2A2] VCC] 2A3 [2A5] 2A6] 2A7]	V, OR D (TOP VI) 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22 22	L P EW 56 55 54 53 52 51 50 49 48 47 46 54 43 42 41 40 38 37 36 35 4	ACKAGE 10E 10E 10E 10E 10E 10E 10E 10	
2A5 [2A6 [21 22	36 35	2B5 2B6	
2A4 [2A5] 2A6]	20 21 22	36 35	2B5 2B5 2B6	
2A7 [2A8 [23 24	34 33	2B7 2B8	
2A9 [2A10 [2A11 [25 26 27	32 31 30	2B9 2B10 2B11	
2A12 [28	29	2B12	

NC - No internal connection



SCDS028H - JULY 1995 - REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	V to 7 V
Input voltage range, V _I (see Note 1)		-0.5	V to 7 V $\!\!\!$
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		.65°C 1	to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITI	ONS	MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V	
1.		$V_{CC} = 0 V,$	V _I = 5.5 V				10		
1		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA	
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA	
∆lcc‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA	
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				3		pF	
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			5.5		pF	
r _{on} §		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		14	20		
			$V_{\rm L} = 0$	lj = 64 mA		5	7	Ω	
		V _{CC} = 4.5 V	vi - 0	lı = 30 mA		5	7		
			$V_{l} = 2.4 V,$	lj = 15 mA		8	12		

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO	V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT
		(001201)	MIN MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A	0.35		0.25	ns
ten	ŌĒ	A or B	9.3	3.3	8.6	ns
^t dis	OE	A or B	7.1	2.8	7.9	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS028H – JULY 1995 – REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SN74CBTH16211 24-BIT FET BUS SWITCH WITH BUS HOLD

- REVISED OCTOBER 1998

	SCDS062A – JUI	WIIH NE 1998 – REVIS
 5-Ω Switch Connection Between Two Ports TTL-Compatible Input Levels 	DGG, DGV, OR (TOP \	DL PACKAGE /IEW)
 Bus Hold on Data Inputs/Outputs Eliminates the Need for External Pullup/Pulldown Resistors 	NC [1 1A1 [2	56] 1 <u>OE</u> 55] 2 <u>OE</u>
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very 	1A2 U 3 1A3 U 4 1A4 U 5 1A5 U 6	54 1B1 53 1B2 52 1B3 51 1B4
Small-Outline (DGV) Packages	1A6 [7 GND [8	50] 1B5 49] GND
The SN74CBTH16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay	1A7 [9 1A8 [10 1A9 [11 1A10 [12 1A11 [13 1A12 [14	48] 1B6 47] 1B7 46] 1B8 45] 1B9 44] 1B10 43] 1B11
The device is organized as dual 12-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 12-bit bus switches or one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch	2A1 [15 2A2 [16 V _{CC} [17 2A3 [18 GND [19 2A4 [20 2A5 [21	42] 1B12 41] 2B1 40] 2B2 39] 2B3 38] GND 37] 2B4 26] 2B5
is open, and a high-impedance state exists between the two ports.	2A3 [21 2A6 [22 2A7 [23	35 2B5 35 2B6 34 2B7
Active bus-hold circuitry is provided to hold unused or floating A and B ports at a valid logic	2A8 🚺 24 2A9 🚺 25	33 2B8 32 2B9

level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTH16211 is characterized for operation from -40°C to 85°C.

> FUNCTION TABLE (each bus switch)

2A10 🛛 26

2A11 27

28

NC - No internal connection

2A12

31 2B10

30 2B11

29 2B12

	FUNCTION		
L	A port = B port		
н	Disconnect		

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN74CBTH16211 24-BIT FET BUS SWITCH WITH BUS HOLD

SCDS062A - JUNE 1998 - REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	V to 7 V
Input voltage range, V _I (see Note 1)		-0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		-65°C t	to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C
				·

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN74CBTH16211 24-BIT FET BUS SWITCH WITH BUS HOLD SCDS062A - JUNE 1998 - REVISED OCTOBER 1998

TEST CONDITIONS TYP[†] PARAMETER MIN MAX UNIT $V_{CC} = 4.5 V,$ -1.2 V VIK $I_{I} = -18 \text{ mA}$ VI = 5.5 V ±10 Control inputs $V_{CC} = 0 V,$ h μΑ V_{CC} = 5.5 V, All inputs $V_I = 5.5 V \text{ or GND}$ ±10 I_{BHL}‡ V_{CC} = 4.5 V, $V_{I} = 0.8 V$ 100 μA -100 IBHH§ $V_{CC} = 4.5 V_{,}$ $V_I = 2 V$ μΑ 500 V_{CC} = 5.5 V, $V_{I} = 0$ to 5.5 V **IBHLO** μΑ -500 ^Івнно[#] $V_{CC} = 5.5 V_{,}$ $V_{I} = 0$ to 5.5 V μΑ V_{CC} = 5.5 V, $V_I = V_{CC} \text{ or } GND$ 3 μΑ ICC $I_{O} = 0$, Control inputs V_{CC} = 5.5 V, 2.5 ∆ICC One input at 3.4 V, Other inputs at V_{CC} or GND mΑ $V_{CC} = 4 V,$ $V_{I} = 2.4 V,$ $I_{I} = 15 \text{ mA}$ 14 20 TYP at V_{CC} = 4 V $I_I = 64 \text{ mA}$ 5 7 ron☆ Ω $V_I = 0$ $V_{CC} = 4.5 V$ 7 $I_I = 30 \text{ mA}$ 5 12 $V_{I} = 2.4 V_{,}$ $I_{I} = 15 \text{ mA}$ 8

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to VII max.

§ The bus hold circuit can source at least the minimum high sustaining current at VIH min. IBHH should be measured after raising VIN to VCC and then lowering it to VIH min.

 \P An external driver must source at least I_{BHLO} to switch this node from low to high.

[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.

I This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

*Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT
		(001101)	MIN MAX	MIN	MAX	
tpd□	A or B	B or A	0.35		0.25	ns
ten	ŌĒ	A or B	9.9	1	9.6	ns
tdis	ŌĒ	A or B	9.5	1	8.3	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS062A - JUNE 1998 - REVISED OCTOBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_r ≤ 2.5 ns, t_r ≤ 2.5 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.





SCDS073 - JULY 1998

 25-Ω Switch Connection Between Two Ports 	DGG, DGV, OR (TOP \	DL PACKAGE /IEW)
TTL-Compatible Input Levels		
 Package Options Include Plastic 300-mil 		56] 10E
Shrink Small-Outline (DL). Thin Shrink		55 U 20E
Small-Outline (DGG), and Thin Very		54 J 1B1
Small-Outline (DGV) Packages		53 J 1B2
		52 J 1B3
description		51 104
The SN/4CBTR16211 provides 24 bits of		
nign-speed TTL-compatible bus switching. The		40 1 B0 47 1 1 B7
low on-state resistance of the switch allows		47 U 1B7 46 U 1B8
dolay		40 1 1 B0 45 1 1 B0
uelay.		43 U 1B3
The device operates as a dual 12- <u>bit</u> bus switch or		44 U 1B10 43 U 1B11
single 24-bit bus switch. Whe <u>n 1</u> OE is low, 1A is		43 1 1B12
connected to 1B. When 2OE is low, 2A is	2A2 116	41 0 2B1
connected to 2B.	Voc 17	4012B2
The device has equivalent 25- Ω series resistors to	2A3 [] 18	39 2B3
reduce signal-reflection noise. This eliminates the	GND [19	38 I GND
need for external terminating resistors.	2A4 [20	37 12B4
	2A5 [21	3612B5
The SIV/40BTR16211 IS Characterized for	2A6 122	35 1 2B6
$operation nom -40^{\circ} C to 85^{\circ} C.$	2A7 123	34 1 2B7
FUNCTION TABLE	2A8 24	33 1 2B8
(each 12-bit bus switch)	2A9 25	32 1 2B9
INPUTS INPUTS/OUTPUTS	2A10 26	31 2B10

INP	UTS	INPUTS/0	OUTPUTS
10E	2OE	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	Н	1A = 1B	Z
н	L	Z	2A = 2B
н	Н	Z	Z

NC - No internal connection

30 2B11

29 2B12

2A11 27

2A12 28

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SCDS073 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	√ to 7 V
Continuous channel current		-0.5	128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2)	: DGG package	4	81°C/W
- · · · · · · · · · · · · · · · · · · ·	DGV package	3	86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		65°C to	o 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCDS073 - JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT		
VIK		$V_{CC} = 4.5 V,$	l _l = –18 mA				-1.2	V	
lı		$V_{CC} = 0 V,$	VI = 5.5 V				10	μA	
		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1		
ICC		V _{CC} = 5.5 V,	IO = 0,	$V_I = V_{CC}$ or GND			3	μA	
∆lCC‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA	
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$						pF	
Cio(OFF)	1	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF	
r _{on} §		V _{CC} = 4.5 V	$\lambda t_{\rm r} = 0$	l _l = 64 mA					
			V] = 0	lı = 30 mA				Ω	
			$V_1 = 2.4 V_2$	lı = 15 mA					

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
^t pd¶	A or B	B or A		ns
^t en	OE	A or B		ns
^t dis	ŌĒ	A or B		ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS073 - JULY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SN54CBT16212A . . . WD PACKAGE SN74CBT16212A . . . DGG, DGV, OR DL PACKAGE

(TOD VIEW)

SCDS007M - NOVEMBER 1992 - REVISED SEPTEMBER 1998

- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages, and Ceramic Flat (WD) Package

description

The 'CBT16212A devices provide 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Each device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

The SN54CBT16212A is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74CBT16212A is characterized for operation from -40° C to 85° C.

	(101	vi L vv)	
,		\mathcal{T}	-
S0	1	56	J S1
1A1	2	55	S2
1A2	3	54	1B1
2A1	4	53	1B2
2A2	5	52	2B1
3A1	6	51] 2B2
3A2	7	50	3B1
GND	8	49] GND
4A1	9	48	3B2
4A2	10	47	4B1
5A1	11	46	4B2
5A2	12	45	5B1
6A1	13	44	5B2
6A2	14	43	6B1
7A1	15	42	6B2
7A2	16	41] 7B1
V _{CC}	17	40	7B2
8A1	18	39	8B1
GND	19	38] GND
8A2	20	37	8B2
9A1	21	36	9B1
9A2	22	35	9B2
10A1	23	34] 10B1
10A2	24	33	10B2
11A1	25	32] 11B1
11A2	26	31] 11B2
12A1	27	30] 12B1
12A2	28	29] 12B2

INPUTS			INPUTS/0	OUTPUTS	FUNCTION
S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	Н	B1 port	Z	A1 port = B1 port
L	Н	L	B2 port	Z	A1 port = B2 port
L	н	Н	Z	B1 port	A2 port = B1 port
н	L	L	Z	B2 port	A2 port = B2 port
Н	L	Н	Z	Z	Disconnect
Н	н	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
Н	Н	н	B2 port	B1 port	A1 port = B2 port A2 port = B1 port

FUNCTION TABLE

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1998, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SCDS007M - NOVEMBER 1992 - REVISED SEPTEMBER 1998

logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, and DL packages.



SCDS007M - NOVEMBER 1992 - REVISED SEPTEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, IIK (VI < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		–65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54CBT	16212A	SN74CBT	16212A	
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	4	5.5	V
VIH	High-level control input voltage	2		2		V
VIL	Low-level control input voltage		0.8		0.8	V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CON			SN54CBT16212A SN74CBT16212			212A					
					MIN	TYP‡	MAX	MIN	түр‡	MAX	UNIT		
VIK		V _{CC} = 4.5 V,	lj = –18 mA				-1.2			-1.2	V		
		$V_{CC} = 0,$	V _I = 5.5 V				10			10			
1		V _{CC} = 5.5 V,	V _I = 5.5 V o	r GND			±1			±1	μΑ		
lcc		$V_{CC} = 5.5 V,$ $V_I = V_{CC} \text{ or GND}$	I _O = 0,		$C = 5.5 \text{ V},$ $I_{O} = 0,$ = V _{CC} or GND		3.2		3.2			3	μΑ
∆ICC§	Control inputs	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				2.5			2.5	mA		
Ci	Control inputs	V _I = 3 V or 0				2.5			2.5		pF		
C _{io(OFF}	-)	V _O = 3 V or 0,	S0, S1, or S	2 = V _{CC}		7.5			7.5		pF		
		$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lı = 15 mA		14	20		14	20			
ron¶			$V_{\rm b} = 0$	lı = 64 mA		4	10		4	7	Ω		
		V _{CC} = 4.5 V	v] = 0	lj = 30 mA		4	10		4	7			
			V _I = 2.4 V,	lj = 15 mA		6	14		6	12			

[‡] All typical values are at $V_{CC} = 5 V$ (unless otherwise noted), $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SCDS007M - NOVEMBER 1992 - REVISED SEPTEMBER 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

			S	N54CB	T16212A		S	SN74CBT16212A			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} :	= 4 V	: V _{CC} ± 0	= 5 V 5 V	V _{CC} =	= 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tpd [†]	A or B	B or A				0.8*		0.35		0.25	ns
^t pd	S	A or B		14	1.5	13		10	1.5	9.1	ns
t _{en}	S	A or B		15	1.5	13.7		10.4	1.5	9.7	ns
tdis	S	A or B		14.2	1.5	13.5		9.2	1.5	8.8	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



- NOTES: A. $\ensuremath{\mathsf{C}}_L$ includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .





SN74CBTR16212 24-BIT FET BUS-EXCHANGE SWITCH

SCDS074 - JULY 1998

 25-Ω Switch Connection Between Two Ports 	DGG, DG	ev, or dl f (top view	PACKAGE ')
TTL-Compatible Input Levels		$\int \nabla z$	h_{α}
Package Options Include Plastic Thin			
Shrink Small-Outline (DGG), Thin Very		2 55	
Small-Outline (DGV), and 300-mil Shrink	241	5 04 4 52	
Small-Outline (DL) Packages	247	5 52	
	3A1	6 51	
description	3A2	7 50	1 3B1
The SN71CBTR16212 provides 21 bits of	GND	8 49	
high-speed TTL-compatible bus switching or	4A1	9 48	5 3B2
exchanging The low on-state resistance of the	4A2	10 47	6 4B1
switch allows connections to be made with	5A1	11 46	4 B2
minimal propagation delay.	5A2	12 45	5B1
The device exercise on a 24 hit hue ewitch or a	6A1	13 44	5B2
12 bit hun exchanger which provides date	6A2	14 43	6B1
avebanging between the four signal ports via the	7A1 🛛	15 42	6 B2
data-select (S0-S2) terminals	7A2	16 41] 7B1
	V _{CC}	17 40	7 B2
The device has equivalent 25- Ω series resistors to	8A1 🛛	18 39	8 B1
reduce signal-reflection noise. This eliminates the	GND 🛛	19 38	GND
need for external terminating resistors.	8A2	20 37	8B2
The SN74CBTR16212 is characterized for	9A1 [21 36	9B1
operation from -40°C to 85°C.	9A2	22 35	9B2
•	10A1 [23 34	10B1
	10A2	24 33	10B2
	11A1 L	25 32	U 11B1
	11A2	26 31	U 11B2
	12A1 [27 30	L 12B1
	12A2	28 29	∐ 12B2

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FUNCTION TABLE								
	INPUTS		INPUTS/0	OUTPUTS	EUNCTION			
S2	S1	S0	A1	A2	FUNCTION			
L	L	L	Z	Z	Disconnect			
L	L	Н	B1 port	Z	A1 port = B1 port			
L	н	L	B2 port	Z	A1 port = B2 port			
L	н	Н	Z	B1 port	A2 port = B1 port			
Н	L	L	Z	B2 port	A2 port = B2 port			
Н	L	Н	Z	Z	Disconnect			
Н	н	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port			
н	Н	н	B2 port	B1 port	A1 port = B2 port A2 port = B1 port			

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

SN74CBTR16212 24-BIT FET BUS-EXCHANGE SWITCH

SCDS074 - JULY 1998

logic diagram (positive logic)




SCDS074 - JULY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I_{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		-65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C
NOTE A				

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
ų		$V_{CC} = 0,$	V _I = 5.5 V				10	
		V _{CC} = 5.5 V,	$V_{I} = 5.5 \text{ V or GND}$				±1	μΑ
Icc		V _{CC} = 5.5 V,	lO = 0,	$V_I = V_{CC}$ or GND			3	μΑ
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V, Other inputs at V _{CC} or GND				2.5	mA
Ci	Control inputs	V _I = 3 V or 0						pF
Cio(OFF)		V _O = 3 V or 0,	S0, S1, or S2 = V_{CC}	;				pF
ron¶				lj = 64 mA				
		$V_{CC} = 4.5 V$	VI = 0	lı = 30 mA				Ω
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SCDS074 - JULY 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} †	A or B	B or A		ns
^t pd	S	A or B		ns
ten	S	A or B		ns
^t dis	S	A or B		ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.





SCDS026F - MAY 1995 - REVISED MAY 1998

- **5**-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBT16213 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN74CBT16213 is characterized for operation from -40° C to 85°C.

DGG, DGV, OR DL PACKAGE					
	(TOP VI	EW)		
-			L		
S0 L	1	56	LS1		
1A1 L	2	55	S2		
1A2 L	3	54	1B1		
2A1 L	4	53	1B2		
2A2 L	5	52	2B1		
3A1 L	6	51	2B2		
3A2 🛓	7	50	3B1		
GND	8	49	GND		
4A1 🛛	9	48	3B2		
4A2 🛛	10	47	4B1		
5A1 🛛	11	46	4B2		
5A2	12	45	5B1		
6A1 🛛	13	44	5B2		
6A2	14	43	6B1		
7A1 [15	42	6B2		
7A2	16	41	7B1		
V _{CC}	17	40	7B2		
8A1 [18	39	8B1		
GND [19	38	GND		
8A2 [20	37	8B2		
9A1 [21	36	9B1		
9A2 [22	35	9B2		
10A1 [23	34	10B1		
10A2 🛛	24	33	10B2		
11A1 [25	32	11B1		
11A2 [26	31	11B2		
12A1 [27	30	12B1		
12A2 🛛	28	29	12B2		

	INPUTS		INPUTS/OUTPUTS		FUNCTION
S2	S 1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	н	B1	Z	A1 port = B1 port
L	Н	L	B2	Z	A1 port = B2 port
L	н	н	Z	B1	A2 port = B1 port
н	L	L	Z	B2	A2 port = B2 port
н	L	Н	A2 and B2	A1 and B2	A1 port = A2 port = B2 port
н	Н	L	B1	B2	A1 port = B1 port A2 port = B2 port
н	н	Н	B2	B1	A1 port = B2 port A2 port = B1 port

FUNCTION TABLE

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SCDS026F - MAY 1995 - REVISED MAY 1998

logic diagram (positive logic)





SCDS026F - MAY 1995 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

V _{CC} Supply voltage 4	5.5	V
V _{IH} High-level control input voltage 2		V
VIL Low-level control input voltage	0.8	V
T _A Operating free-air temperature -40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
1.		$V_{CC} = 0,$	V _I = 5.5 V				10	
ч 		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				4.5		pF
C _{io(OFF)}	B port		S0, S1, or S2 = V _{CC}			8.5		~ F
	A port	vO = 3 v or 0,				8		рг
	A to B or B to A $V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$ $V_{CC} = 4.5 V$	$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		14	20	
		B or	V. 0	lı = 64 mA		5	7	
		$V_{\rm CC} = 4.5 \text{V}$	VI = 0	lı = 30 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		8	15	0
ron [¶]		$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		22	30	52
	A1 to A2		V/- 0	lı = 64 mA		10	14	
		$V_{CC} = 4.5 V$	v] = 0	lı = 30 mA		10	14	
			V _I = 2.4 V,	lj = 15 mA		16	22	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SCDS026F - MAY 1995 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTBUT)	V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT	
	(MIN MAX	MIN	MAX		
t _{pd} †	A or B	B or A	0.35		0.25		
	A1	A2	0.5		0.5	ns	
t _{en}	S	A or B	12.4	3.2	11.1	ns	
^t dis	S	A or B	12.4	2.3	11.9	ns	
t _{en}	S0	A2 and B2	11.5	4	10.9	ns	
^t dis	SO	A2 and B2	12.8	5.7	12	ns	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tp71 and tp7H are the same as t_{en} .
- G. tpLH and tpHL are the same as t_{pd} .





SCDS008I - MAY 1993 - REVISED MAY 1998

 5-Ω Switch Connection Between Two Ports TTL-Compatible Input Levels 	DGG OR DL PACKAGE (TOP VIEW)			
 Package Options Include Plastic Thin 	SOL		56151	
Shrink Small-Outline (DGG) and 300-mil	1АП	2	55 I S2	
Shrink Small-Outline (DL) Packages	1B3	3	54 1B1	
	2A 🛛	4	53 🛛 1B2	
description	2B3 🛛	5	52 2B1	
The SN74CBT16214 provides 12 bits of	3A [6	51 2B2	
high-speed TTL-compatible bus switching	3B3 [7	50 3B1	
between three separate ports. The low on-state	GND [8	49] GND	
resistance of the switch allows connections to be	4A [9	48] 3B2	
made with minimal propagation delay.	4B3 [10	47] 4B1	
The device energies of a 12 bit bus calent switch	5A 🛛	11	46] 4B2	
via the data-select (S0-S2) terminals	5B3 🛛	12	45 5 B1	
	6A [13	44] 5B2	
The SN74CBT16214 is characterized for	6B3 🛛	14	43 6B1	
operation from –40°C to 85°C.	7A [15	42 0 6B2	
	7B3 🛛	16	41 7 7B1	
	Vcc [17	40 7 B2	
	8A []	18	39 8B1	
	GND [19	38 GND	
	8B3 🛛	20	37 8B2	
	9A [21	36 9B1	
	9B3 [22	35 9B2	
	10A 🛛	23	34 01 10B1	
	10B3	24	33 10B2	
	11A 🛛	25	32 11B1	
	11B3 🛛	26	31 🛛 11B2	

	FUNCTION TABLE								
INPUTS			INPUT/OUTPUT	FUNCTION					
S2	S1	S0	A	FUNCTION					
L	L	L	Z	Disconnect					
L	L	Н	B1	A port = B1 port					
L	Н	L	B2	A port = B2 port					
L	н	н	Z	Disconnect					
н	L	L	Z	Disconnect					
Н	L	Н	B3	A port = B3 port					
Н	Н	L	B1	A port = B1 port					
н	н	н	B2	A port = B2 port					

I



30 12B1

29 🛛 12B2

12A 🛛 27 12B3 🚺 28

SCDS008I - MAY 1993 - REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		-0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, IIK (VI < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	81°C
	DL package	74°C
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



SCDS008I - MAY 1993 - REVISED MAY 1998

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER		TEST CONDITION	ONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
		$V_{CC} = 0,$	V _I = 5.5 V				10	
I II		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆lcc‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				4		pF
Cio(OFF)		V _O = 3 V or 0,	A = Z			7.5		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA				
ron§			V/I – 0	lj = 64 mA		4	7	Ω
		$V_{CC} = 4.5 V$	VI = 0	lı = 30 mA		4	7	
			V _I = 2.4 V,	lj = 15 mA		6	12	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTRUT)	V _{CC} =	= 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
		(001101)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.35		0.25	ns
^t pd	S	B or A		15.3	5.5	13.9	ns
ten	S	A or B		16	5.1	14.5	ns
^t dis	S	A or B		12.1	3.6	11.7	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS008I - MAY 1993 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBT16232 SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

Y 1995 – REVISED OCTOBER 1998

DGG OR	DL PACKAGE
(1)	OP VIEW)
1A [1 2B1 [2 2B2 [3 3A [4	56] 1B1 55] 1B2 54] 2A 53] 3B1
4B1 5	52 1 3B2
4B2 [6 5A [7 6B1 [8 6B2 [9 7A [10 8B1 [11	51] 4A 50] 5B1 49] 5B2 48] 6A 0 47] 7B1 46] 7B2
662 [] 12 GND [] 13 V _{CC} [] 14 9A [] 15 10B1 [] 16	2 43 6A 3 44 GNI 4 43 V _{CC} 5 42 9B1 6 41 9B2
10B2 [] 17 11A [] 18 12B1 [] 19 12B2 [] 20 13A [] 22 14B1 [] 22 14B2 [] 24 15A [] 24	7 40 10A 3 39 11B 9 38 11B 9 38 12A 1 36 13B 2 35 13B 2 35 13B 3 34 14A 4 33 15B
	1A [1 2B1 [2 2B2 [3 3A [4 4B1 [5 4B2 [6 5A [7 6B1 [8 6B2 [9 7A [10 8B1 [12 8B2 [12 GND [12 V _{CC} [14 10B1 [10 10B2 [17 11A [18 12B1 [12 12B2 [20 13A [22 14B1 [22 14B1 [22 15A [24 16B1 [25

4B1 [5	52	3B2
4B2 🛛	6	51] 4A
5A 🗌	7	50] 5B1
6B1 [8	49	5B2
6B2 🛛	9	48	6A
7A [10	47	7B1
8B1 [11	46	7B2
8B2 [12	45	8A
GND [13	44	GND
Vcc [14	43	Vcc
9A [15	42	9B1
10B1	16	41	9B2
10B2	17	40	10A
11A 🛛	18	39	11B1
12B1	19	38] 11B2
12B2	20	37	12A
13A 🛛	21	36	0 13B1
14B1	22	35] 13B2
14B2	23	34	14A
15A 🛛	24	33	15B1
16B1	25	32	15B2
16B2	26	31	16A
CLK	27	30	S 0
CLKEN	28	29	S1
_			

FUNCTION TABLE

	INF	PUTS	FUNCTION	
S1	S0	CLK	CLKEN	FUNCTION
Х	Х	Х	Н	Last state
L	L	\uparrow	L	Disconnect
L	Н	\uparrow	L	A = B1 and A = B2
н	L	\uparrow	L	A = B1
н	н	\uparrow	L	A = B2



SN74CBT16232 SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009I - MAY 1995 - REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТĄ	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDIT	IONS		MIN	TYP†	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	l _l = -18 mA					-1.2	V
Ц		$V_{CC} = 5.5 V,$	$V_{I} = 5.5 V \text{ or GND}$					±1	μΑ
ICC		$V_{CC} = 5.5 V,$	I _O = 0,	$V_{I} = V_{CC} \text{ or } GN$	ND			3	μA
$\Delta I C C^{\ddagger}$	Control inputs	$V_{CC} = 5.5 V,$	One input at 3.4 V,	Other inputs at	V _{CC} or GND			2.5	mA
Ci	Control inputs	$V_I = 3 V \text{ or } 0$					4.5		pF
	A port		$\overline{\text{CLKEN}} = 0,$	S0 = 0, S1 = 0	0 4		6.5		<u>م</u> ۲
Cio(OFF)	B port	$V_{O} = 3 V \text{ or } 0,$			S1 = 0		4		рг
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	l _l = 15 mA			14	20	
r _{on} §			$\mathcal{V}_{t} = 0$	l _l = 64 mA			5	7	Ω
		$V_{CC} = 4.5 V$	v] = 0	I _I = 30 mA			5	7	
			V _I = 2.4 V,	lı = 15 mA			10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER					V _{CC} = 5 V ± 0.5 V	
				MAX	MIN	MAX	
fclock	Clock frequency			150		150	MHz
tw	Pulse duration	CLK high or low	3.3		3.3		ns
+	Cature time	S0, S1 before CLK↑	2.2		1.9		20
^t su s	Setup time	CLKEN before CLK↑	2.4		1.9		ns
+.		S0, S1 after CLK↑	0.5		1		20
ĥ		CLKEN after CLK [↑]	1.9		1.8		115

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTRUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
t _{pd} ¶	A or B	B or A		0.35		0.25	ns
^t pd	CLK	A or B		6.1	2	5.8	ns
	CLK	A, B1, B2		6.8	1.8	6.2	20
len		B1 or B2		8.5	3.1	7.9	ns
tdis	CLK	A or B		5.8	1.9	6.2	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBT16232 SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009I - MAY 1995 - REVISED OCTOBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS010H - MAY 1995 - REVISED OCTOBER 1998

 5-Ω Switch Connection Between Two Ports TTL-Compatible Input Levels 	DGG, DGV, OR DL PACKAGE (TOP VIEW)			
 Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages 	1A [₁ 56] 1B1 2B1 [2 55] 1B2 2B2 [3 54] 2A 3A [4 53] 3B1			
description	4B1 5 52 3B2 4B2 6 51 4 A			
The SN74CBT16233 is a 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The device can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer	5A 7 50 5B1 6B1 8 49 5B2 6B2 9 48 6A 7A 10 47 7B1 8B1 11 46 7B2 8B2 12 45 8A GND 13 44 GND V _{CC} 14 43 V _{CC} 9A 15 42 9B1			
Two select (SEL1 and SEL2) inputs control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.	10B1 16 41 9B2 10B2 17 40 10A 11A 18 39 11B1 12B1 19 38 11B2 12B2 20 37 12A 13A 21 36 13B1 14B1 22 35 13B2			
The device is specified by design not to have through current when switching directions. The SN74CBT16233 is characterized for operation from 0°C to 70°C.	14B2 23 34 14A 15A 24 33 15B1 16B1 25 32 15B2 16B2 26 31 16A TEST1 27 30 SEL1 TEST2 28 29 SEL2			

FUNCTION TABLE (each multiplexer/demultiplexer)

INP	UTS	FUNCTION
SEL	TEST	FUNCTION
L	L	A = B1
н	L	A = B2
х	н	A = B1 and A = B2



SCDS010H - MAY 1995 - REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, VI (see Note 1)		. –0.5 V to V _{CC} + 0.5 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC} Suppl	y voltage	4.75	5.25	V
VIH High-	evel control input voltage	2		V
VIL Low-le	evel control input voltage		0.8	V
T _A Opera	ting free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS		IONS	MIN	TYP†	MAX	UNIT		
VIK		V _{CC} = 4.75 V,	l _l = –18 mA				-1.2	V
		$V_{CC} = 0,$	V _I = 5.25 V				10	μA
'I		V _{CC} = 5.25 V,	$V_I = 5.25 \text{ V or GND}$				±1	μA
ICC		V _{CC} = 5.25 V,	IO = 0,	$V_{I} = V_{CC} \text{ or } GND$			3	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				4.5		pF
Cio(OFF))	$V_{O} = 3 V \text{ or } 0$				4		pF
			$\lambda = 0$	l _l = 64 mA		5	7	
r _{on} §		V _{CC} = 4.75 V	V] = 0	l _l = 30 mA		5	7	Ω
			$V_{I} = 2.4 V_{,}$	lı = 15 mA		7	12	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A		0.25	ns
^t pd	SEL	A	1.6	5.3	ns
t _{en}	TEST or SEL	В	1.3	5.2	ns
t _{dis}	TEST or SEL	В	1	5.3	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SCDS075A - JULY 1998 - REVISED OCTOBER 1998

 25-Ω Switch Connection Between Two Ports 	DGG, DGV, OR DL PACKAGE (TOP VIEW)
TTL-Compatible Input Levels	
 Package Options Include Plastic Thin 	
Shrink Small-Outline (DGG). Thin Verv	
Small-Outline (DGV), and 300-mil Shrink	$3 \Delta \Pi_{4}$ $\epsilon_{2} \Pi_{3} R_{1}$
Small-Outline (DL) Packages	$4B1\Pi_{5}$ 53[1007 $4B1\Pi_{5}$ 52[13B2
	$4B_2 \Pi_6$ $52 \Pi_{0} D_2$
description	$54\Pi_7$ 501581
	6B1 De 40 D5B2
The SN/4CBTR16233 is a 16-bit 1-of-2 FET	
multiplexer/demultiplexer used in applications in	
which two separate data paths must be	8B1 11 46 7B2
nulliplexed onlo, of demulliplexed from, a single	8B2 1 12 45 1 8A
interleaving where two different banks of memory	
need to be addressed simultaneously. The device	
can be used as two 8-bit to 16-bit multiplevers or	9A I 15 42 I 9B1
as one 16-bit to 32-bit multiplexer	10B1 116 41 19B2
	10B2 1 17 40 1 10A
Two select (SEL1 and SEL2) inputs control the	
data flow. When the TEST inputs are asserted, the	12B1 19 38 11B2
A port is connected to both the B1 and the B2	12B2 120 37 112A
ports. SEL1, SEL2, and the TEST inputs can be	13A [21 36] 13B1
driven with a 5-V CMOS, a 5-V IIL, or a	14B1 22 35 13B2
low-voltage IIL driver.	14B2 23 34 14A
The SN74CBTR16233 is specified by design not	15A 24 33 15B1
to have through current when switching	16B1 25 32 15B2
directions.	16B2 26 31 16A
The device has equivalent 25-0 series resistors to	TEST1 27 30 SEL1
reduce signal-reflection noise. This eliminates the	TEST2 28 29 SEL2
need for external terminating resistors.	1ſ

The SN74CBTR16233 is characterized for operation from 0° C to 70° C.

FUNCTION TABLE
(each multiplexer/demultiplexer)

INP	UTS	FUNCTION		
SEL	TEST	FUNCTION		
L	L	A = B1		
н	L	A = B2		
Х	Н	A = B1 and A = B2		



SCDS075A - JULY 1998 - REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		-0.5 V to V _{CC} + 0.5 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		\ldots –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.25	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТĄ	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	PARAMETER TEST CONDITIONS		MIN	түр†	MAX	UNIT		
VIK		V _{CC} = 4.75 V,	l _l = –18 mA				-1.2	V
		$V_{CC} = 0,$	V _I = 5.25 V				10	μΑ
<u>ч</u>		V _{CC} = 5.25 V,	V _I = 5.25 V or GND				±1	μÂ
ICC		V _{CC} = 5.25 V,	IO = 0,	$V_{I} = V_{CC} \text{ or } GND$			3	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$						pF
Cio(OFF))	$V_{O} = 3 V \text{ or } 0$						pF
ron§			$\lambda = 0$	l _l = 64 mA				
		V _{CC} = 4.75 V	vj=0	II = 30 mA				Ω
			$V_1 = 2.4 V_2$	lı = 15 mA				

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	мах	UNIT
t _{pd} ¶	A or B	B or A			ns
^t pd	SEL	A			ns
^t en	TEST or SEL	В			ns
^t dis	TEST or SEL	В			ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS075A - JULY 1998 - REVISED OCTOBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

E. tPLZ and tPHZ are the same as tdis.

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS031G - MAY 1996 - REVISED SEPTEMBER 1998

- Standard '16244-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages, and Ceramic Flat (WD) Package

description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN54CBT16244 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74CBT16244 is characterized for operation from -40° C to 85° C.

SN54CBT1	6244	WD PACKAGE
SN74CBT16244	. DGG, I	DGV, OR DL PACKAGE
	(TOP VI	EW)
r	\cup	┓_
10E L	1 -	48 U 20E
1B1 L	2	47 1 1A1
1B2	3	46 1A2
GND	4	45 GND
1B3 [5	44 1A3
1B4 🛛	6	43 AA4
v _{cc} [7	42 V _{CC}
2B1	8	41 2A1
2B2	9	40 2A2
GND 🛛	10	39 GND
2B3 🛛	11	38 2A3
2B4 🛛	12	37 2A4
3B1 🛛	13	36 3A1
3B2	14	35 3A2
GND	15	34 GND
3B3 🛛	16	33 3A3
3B4 🛛	17	32 3A4
Vcc	18	31 V _{CC}
4B1	19	30 4A1
4B2	20	29 4A2
GND	21	28 GND
4B3 🛛	22	27 🛛 4A3
4B4 🛛	23	26 4 A4
4 <u>0</u> [24	25 30E

FUNCTION TABLE (each 4-bit bus switch)

(04011 1 210 240 01110							
	OUTPUTS A, B						
L	A port = B port						
н	Z						

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1998, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SCDS031G - MAY 1996 - REVISED SEPTEMBER 1998

logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, and DL packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	V to 7 V
Input voltage range, V _I (see Note 1)		-0.5	V to 7 V $$
Continuous channel current			128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{stg}		65°C f	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54CBT16244		SN74CB		
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	4	5.5	V
VIH	High-level control input voltage	2		2		V
VIL	Low-level control input voltage		0.8		0.8	V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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	AETED	TEST CONDITIONS			SN5	4CBT16	244	SN74CBT16244			
PARA	VIETER	TEST CON	DITIONS		MIN	түр†	MAX	MIN	түр†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2			-1.2	V
1.		$V_{CC} = 0$	V _I = 5.5 V				10			10	
'1		$V_{CC} = 5.5 V$	V _I = 5.5 V or	GND	±1					±1	μА
ICC		$V_{CC} = 5.5 V,$ $V_{I} = V_{CC} \text{ or GND}$	IO = 0,				3.2			3	μΑ
∆ICC‡	Control inputs	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				2.5			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				2.5			2.5		pF
C _{io(OFF}	-)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = ACC$			4.5			4.5		pF
		$V_{CC} = 4 V,$	V _I = 2.4 V,	l _l = 15 mA			20			20	
- 8			$V_{\rm r} = 0$	l _l = 64 mA		5	10		5	7	0
ⁱ on ³		$V_{CC} = 4.5 V$	V] = 0	l _l = 30 mA		5	10		5	7	52
			V _I = 2.4 V,	lj = 15 mA		8	14		8	12	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. [‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54CB	BT16244			SN74CB	T16244		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} :	= 4 V	۲ <mark>۰۵</mark> کا ۲	= 5 V 5 V	V _{CC}	= 4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A				0.8*		0.35		0.25	ns
ten	ŌĒ	A or B		10.3	1	9.2		5.5	1	5.1	ns
tdis	ŌĒ	A or B		9.7	1	8.2		5.2	1	5.4	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS031G - MAY 1996 - REVISED SEPTEMBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.





SCDS076 - JULY 1998

 Standard '16244-Type Pinout 25-Ω Switch Connection Between Two 	DGG, DGV, OR DL PACKAGE (TOP VIEW)				
Ports	f	$\overline{\mathbf{U}}$	h . 		
TTI -Compatible Input Levels		1 48	1 20E		
Package Ontions Include Plactic Thin		2 47			
Shrink Small-Outline (DGG) Thin Verv		3 46			
Small-Outline (DGV) and 300-mil Shrink		45			
Small-Outline (DOV), and Soo-Inn Shrink Small-Outline (DI) Packages		o 44			
		7 43			
description		42 2 /1			
		0 41			
The SN74CBTR16244 provides 16 bits of		10 39			
high-speed TTL-compatible bus switching in a		10 38			
standard '16244 device pinout. The low on-state	2B3 U 1	12 37			
resistance of the switch allows connections to be	3B1 [] 1	13 36	Δ 2/1		
made with minimal propagation delay.	3B2 [] 1	14 35	1 3A2		
The device is organized as four 4-bit low-impedance		15 34			
switches with separate output-enable (\overline{OE}) inputs.	3B3 [] 1	16 33	3A3		
When OE is low, the switch is on and data can flow	3B4 1	17 32	3A4		
from port A to port B, or vice versa. When OE is		18 31	Vcc		
high, the switch is open and a high-impedance	4B1 1	19 30	4A1		
state exists between the two ports.	4B2 🛛 2	20 29	4A2		
The device has equivalent $25 \cdot \Omega$ series resistors to	GND 2	21 28	GND		
reduce signal-reflection noise. This eliminates the	4B3 🛛 2	22 27	4A3		
need for external terminating resistors.	4B4 🚺 2	23 26	4A4		
The SN74CBTR16244 is characterized for	4 0E [2	24 25] 3 <u>0</u> E		

operation from -40° C to 85° C.

FUNCTION TABLE

(each 4-bit bus switch)							
	OUTPUTS A, B						
L	A port = B port						
н	Z						

PRODUCT PREVIEW



SCDS076 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, VI (see Note 1)		. –0.5	V to 7 V $$
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{stg}		-65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITIONS				MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
		VCC = 0	V _I = 5.5 V				10	
		V _{CC} = 5.5 V	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			3	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{io(OFF})	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
			$\lambda = 0$	l _l = 64 mA				
r _{on} §		V _{CC} = 4.5 V	v] = 0	l _l = 30 mA				Ω
			$V_1 = 2.4 V_2$	lı = 15 mA				

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A			ns
t _{en}	ŌĒ	A or B			ns
^t dis	ŌĒ	A or B			ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS076 - JULY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 M D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{dis} .
- G. tpLH and tpHL are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SCDS070 - JULY 1998

 Standard '16245-Type Pinout 5-Ω Switch Connection Between Two Ports 	DGG, DGV, OR DL PACKAGE (TOP VIEW)
TTL-Compatible Input Levels	
Package Options Include Plastic Thin	1B1 2 47 1A1
Shrink Small-Outline (DGG), Thin Very	1B2 3 46 1A2
Small-Outline (DGV), and Shrink	GND 4 45 GND
Small-Outline (DL) Packages	1B3 🛛 5 🛛 44 🗋 1A3
	1B4 🛛 6 🛛 43 🗋 1A4
description	V _{CC} [] 7 42] V _{CC}
The SN74CBT16245 provides 16 bits of	1B5 🛛 8 🛛 41 🗖 1A5
high-speed TTI -compatible bus switching in a	1B6 9 40 1A6
standard '16245 device pinout. The low on-state	
resistance of the switch allows connections to be	1B7 11 38 1A7
made with minimal propagation delay.	1B8 12 37 1A8
	2B1 13 36 2A1
I ne device is organized as two 8-bit low-impedance switches with constraints $\overline{(\nabla \Gamma)}$ institute	2B2 14 35 2A2
Switches with separate output-enable (OE) inputs.	GND 15 34 GND
from port A to port B, or vice verse, When \overline{OE} is	2B3 L 16 33 L 2A3
high the switch is open and a high-impedance	2B4 U 17 32 U 2A4
state exists between the two ports	
	2B5 L 19 30 L 2A5
The SN74CBT16245 is characterized for	2B6 U 20 29 U 2A6
operation from –40°C to 85°C.	
	2B8 Ц 23 26 Ц 2A8

NC - No internal connection

25 20E

NC 24

FUNCTION TABLE (each 8-bit bus switch)

	FUNCTION
L	A port = B port
н	Disconnect



SCDS070 - JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, VI (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{stg}		-65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCDS070 - JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CONDIT	IONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
		$V_{CC} = 0,$	VI = 5.5 V				10	
'I		V _{CC} = 5.5 V,	$V_{I} = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	IO = 0,	$V_I = V_{CC}$ or GND			3	μA
∆lcc‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{io(OFF})	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
		$V_{CC} = 4 V,$	V _I = 2.4 V,	lj = 15 mA				
- 6			$\lambda t = 0$	lı = 64 mA				0
rons	۱ ³	V _{CC} = 4.5 V	V] = 0	lı = 30 mA				52
			$V_{I} = 2.4 V_{,}$	lj = 15 mA				

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT	
			MIN	MAX	MIN	MAX		
tpd¶	A or B	B or A					ns	
ten	ŌĒ	A or B					ns	
^t dis	OE	A or B					ns	

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS070 - JULY 1998



PARAMETER MEASUREMENT INFORMATION

PRODUCT PREVIEW

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}. G. tPLH and tPHL are the same as tpd.





SCDS077 - JULY 1998

• Standard '16245-Type Pinout	DGG, DGV, OR DL PACKAGE (TOP VIEW)	:
 25-Ω Switch Connection Between Two Ports 		
 TTL-Compatible Input Levels 		
Pastana Ontinga Indu Levels		
 Package Options Include Plastic Thin Shrink Small Outling (DCC). This Very 		
Smith Small-Outline (DGG), Thin very		
Small-Outline (DGV), and Smink Small-Outline (DL) Packages		
Small-Outline (DL) Fackages		
description		
The SN74CBTR16245 provides 16 bits of		
high-speed TTL-compatible bus switching in a		
standard '16245 device pinout. The low on-state		
resistance of the switch allows connections to be		
made with minimal propagation delay.	2B1U13 30U2A1 2B2U14 35U2A2	
The device is organized as two 8-bit low-impedance		
switches with separate output-enable (\overline{OE}) inputs.		
When \overline{OE} is low, the switch is on and data can flow	284 117 32 244	
from port A to port B, or vice versa. When \overline{OE} is		
high, the switch is open and a high-impedance		
state exists between the two ports.	2B6 20 29 2A6	
The device has equivalent 25-0 series resistors to		
reduce signal-reflection noise. This eliminates the	2B7 22 27 2A7	
need for external terminating resistors.	2B8 23 26 2A8	
The SN/4CBTR16245 is characterized for		
operation from -40° C to 85° C.	NO No internal composition	

NC - No internal connection

FUNCTION TABLE (each 8-bit bus switch)

	FUNCTION
L	A port = B port
н	Disconnect

PRODUCT PREVIEW



SCDS077 – JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, VI (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{stg}		-65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.


SN74CBTR16245 16-BIT FET BUS SWITCH

SCDS077 - JULY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			түр†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
1.		VCC = 0	V _I = 5.5 V				10	
_ 'I		V _{CC} = 5.5 V	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			3	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{io(OFF})	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
			$\lambda = 0$	l _l = 64 mA				
r _{on} §		V _{CC} = 4.5 V	v] = 0	l _l = 30 mA				Ω
			$V_1 = 2.4 V_2$	lı = 15 mA				

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A			ns
t _{en}	ŌĒ	A or B			ns
^t dis	ŌĒ	A or B			ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBTR16245 16-BIT FET BUS SWITCH

SCDS077 - JULY 1998



PARAMETER MEASUREMENT INFORMATION

PRODUCT PREVIEW

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as t_{pd} .





SN74CBT16292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS053B – MARCH 1998 – REVISED MAY 1998

- 4-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBT16292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/ demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1 and R_{INT} is connected to port B2. When S is high, port A is connected to port B2 and R_{INT} is connected to port B1.

The SN74CBT16292 is characterized for operation from -40° C to 85° C.

DGG, DGV, OR DL PACKAGE					
s[) 56	Лис		
1 A L	2	55			
NC	3	54	11B1		
2A [4	53]1B2		
NС	5	52			
зАĒ	6	51	2B2		
NC [7	50	3B1		
gnd [8	49	GND		
4A 🛛	9	48	3B2		
лс [10	47]4B1		
5A 🛛	11	46	4B2		
лс [12	45	5B1		
6A [13	44	5B2		
NC [14	43	6B1		
7A 🛛	15	42	6B2		
NC [16	41]7B1		
V _{CC}	17	40	7B2		
8A [18	39	8B1		
GND [19	38	GND		
NC [20	37	8B2		
9A	21	36	9B1		
NC	22	35	9B2		
10A 🛓	23	34	10B1		
NC	24	33	10B2		
11A 🛛	25	32	11B1		
NC	26	31	11B2		
12A	27	30	12B1		
NC [28	29	12B2		

NC - No internal connection

INPUT S	FUNCTION			
L	A port = B1 port R _{INT} = B2 port			
н	A port = B2 port R _{INT} = B1 port			

FUNCTION TABLE



SN74CBT16292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS SCDS053B – MARCH 1998 – REVISED MAY 1998

3CD3033D - MARCH 1998 - REVISED MAT 19

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		-65°C '	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



SN74CBT16292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS053B - MARCH 1998 - REVISED MAY 1998

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CONDITION	ONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA		-1.2		V	
Ц		V _{CC} = 5.5 V,	$V_{I} = V_{CC} \text{ or } GND$				±5	μA
Icc		V _{CC} = 5.5 V,	I _O = 0,	$V_{I} = V_{CC}$ or GND			3	μA
∆lCC [‡]	Control input	V _{CC} = 5.5 V,	One input at 3.4 V, Other inputs at V_{CC} or GND				2.5	mA
Ci	Control input	VI = 3 V or 0				3		pF
C _{io}		$V_{CC} = 0,$	$V_{O} = 3 V \text{ or } 0$			8		pF
		$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lı = 15 mA		10	20	
ron§			V/I – 0	lı = 64 mA		3	7	Ω
		$V_{CC} = 4.5 V$	$V_{CC} = 4.5 V$ $V_{I} = 0$	lı = 30 mA		3	7	
			$V_{I} = 2.4 V,$	lj = 15 mA		5	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

 \pm This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPLIT)		V _{CC} = 4 V	۷ _{CC} ± 0.	V _{CC} = 5 V ± 0.5 V	
		(0011 01)	MIN MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A	0.5		0.25	ns
ten	S	A or B	6.8	1	6	ns
^t dis	S	A or B	7	1	6.3	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION		DESCRIPTION		V _{CC} = 4 V			UNIT
		MIN	MAX	MIN	MAX			
^t mbb [#]	Make-before-break time	0	2	0	2	ns		

[#]The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



SN74CBT16292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS053B - MARCH 1998 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500- Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500-Ω pulldown resistor.
 - C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , $t_{f} \le 2.5$ ns, $t_{f} \le 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis. Z = RINT = 500 Ω
 - F. tpzL and tpzH are the same as ten. Z = RINT = 500 Ω
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBT162292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS SCDS052C - MARCH 1998 - REVISED MAY 1998

- TTL-Compatible Control Input Levels
- Isolation Under Power-Off Conditions
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- A-Port Inputs/Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBT162292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/ demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1 and R_{INT} is connected to port B2. When S is high, port A is connected to port B2 and R_{INT} is connected to port B1.

The A-port inputs/outputs include equivalent $25 \cdot \Omega$ series resistors to reduce overshoot and undershoot.

The SN74CBT162292 is characterized for operation from -40° C to 85°C.

DGG, DGV, OR DL PACKAGE					
	(TOI	P VIEW)		
г		\cup	L		
SL	1	56	LNC		
1A L	2	55	INC		
NC	3	54	1B1		
2A L	4	53	1B2		
NC	5	52	2B1		
3A L	6	51	2B2		
NC	7	50	3B1		
GND	8	49	GND		
4A	9	48	3B2		
NC	10	47	4B1		
5A	11	46	4B2		
NC	12	45	5B1		
6A [13	44	5B2		
NC [14	43	6B1		
7A 🛛	15	42	6B2		
NC [16	41	7B1		
v _{cc} [17	40	7B2		
8A [18	39	8B1		
gnd [19	38	GND		
NC [20	37	8B2		
9A [21	36	9B1		
NC [22	35	9B2		
10A 🛛	23	34	10B1		
NC [24	33	10B2		
11A 🛛	25	32] 11B1		
NC [26	31] 11B2		
12A 🛛	27	30] 12B1		
NC [28	29	12B2		

NC - No internal connection

FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R _{INT} = B2 port
н	A port = B2 port R _{INT} = B1 port



SN74CBT162292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS SCDS052C - MARCH 1998 - REVISED MAY 1998

SCDS052C – MARCH 1998 – REVISED MAY 199

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I_{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		–65°C 1	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



SN74CBT162292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS052C - MARCH 1998 - REVISED MAY 1998

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 5.5 V,	$V_I = V_{CC} \text{ or } GND$				±5	μA
l _{off}		$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 7 \text{ V}$				10	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
$\Delta I C C^{\ddagger}$	Control input	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control input	VI = 3 V or 0				3.5		pF
C _{io}		V _{CC} = 0,	$V_{O} = 3 V \text{ or } 0$			8		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		38	55	
r _{on} §			$\mathcal{M} = 0$	lı = 45 mA		39	63	Ω
		V _{CC} = 4.5 V	v] = 0	II = 30 mA		37	55	
			V _I = 2.4 V,	lj = 15 mA		37	55	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPLIT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
		(001F01)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		1.9		1.85	ns
t _{en}	S	A or B	1	10.7	1	9.5	ns
^t dis	S	A or B	1	10.9	1	9.7	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION		DESCRIPTION		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V	
			MAX	MIN	MAX			
^t mbb [#]	Make-before-break time		2	0	2	ns		

[#]The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



SN74CBT162292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS052C - MARCH 1998 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

- NOTES: A. CI includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500- Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500-Ω pulldown resistor.
 - C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_r \le 2.5 \text{ ns}, t_f \le 2.5 \text{ ns}.$
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as t_{dis} . Z = RINT = 500 Ω .
 - F. tpzL and tpzH are the same as ten. $Z = R_{INT} = 500 \Omega$.
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS035C - OCTOBER 1997 - REVISED OCTOBER 1998

- **5**-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBT16390 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, in which two different banks of memory must be addressed simultaneously. This also can be used to connect or isolate the PCI bus to one or two slots simultaneously.

Two output enables ($\overline{OE1}$ and $\overline{OE2}$) control the data flow. When $\overline{OE1}$ is low, A port is connected to 1B port. When $\overline{OE2}$ is low, A port is connected to 2B port. When both $\overline{OE1}$ and $\overline{OE2}$ are low, the A port is connected to both 1B and 2B ports. The control inputs can be driven with a 5-V CMOS, 5-V TTL, or an LVTTL driver.

The SN74CBT16390 is characterized for operation from –40°C to 85°C.

DGG, DG	V, OR D (TOP VI	er (EW)	ACKAGE
L		-	L
A1 [1	56]1B1
2B1 [2	55]1B2
2B2	3	54] A2
A3 [4	53]1B3
2B3 [5	52]1B4
2B4 [6	51] A4
A5 [7	50] 1B5
2B5 🛛	8	49]1B6
2B6	9	48	A6
A7 [10	47] 1B7
2B7 🛛	11	46	1B8
2B8	12	45	A8
GND [13	44	GND
Vcc	14	43]∨ _{cc}
A9 [15	42] 1B9
2B9	16	41]1B10
2B10	17	40	A10
A11 [18	39]1B11
2B11	19	38]1B12
2B12	20	37	A12
A13	21	36	1B13
2B13	22	35]1B14
2B14	23	34	A14
A15	24	33] 1B15
2B15	25	32]1B16
2B16	26	31	A16
NC [27	30	OE1
NC	28	29	OE2

NC - No internal connection

FUNCTION TABLE

INPUTS		EUNCTION
OE1	OE2	FUNCTION
L	L	A = 1B and $A = 2B$
L	н	A = 1B
н	L	A = 2B
н	н	Isolation

SCDS035C - OCTOBER 1997 - REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		. –0.5 V to V _{CC} + 0.5 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITI	ONS	MIN	TYP†	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	lj = -18 mA				-1.2	V
		$V_{CC} = 0,$	V _I = 5.5 V				10	
1		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	IO = 0,	$V_I = V_{CC}$ or GND			3	μA
∆lcc‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other input at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				5		pF
C _{io(OFF})	$V_{O} = 3 V \text{ or } 0$				5.5		pF
			$\lambda t_{\rm r} = 0$	lj = 64 mA		5	7	
r _{on} §		$V_{CC} = 4.5 V$	vj=0	l _l = 30 mA		5	7	Ω
			$V_{I} = 2.4 V_{,}$	lı = 15 mA		7	12	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A		0.25	ns
t _{en}	ŌĒ	A or B	1.3	5.9	ns
^t dis	ŌĒ	A or B	1	5.3	ns

The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



SCDS035C - OCTOBER 1997 - REVISED OCTOBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.





SCDS068 - JULY 1998

- **5**-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Shrink Small-Outline (DL) Packages

description

The SN74CBT16861 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one dual 10-bit switch with separate output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

The SN74CBT16861 is characterized for operation from -40° C to 85° C.

DGG OR DL PACKAGE (TOP VIEW)				
DGG NC [1A1 [1A2 [1A3 [1A4 [1A5 [1A6 [1A7 [1A7 [1A7 [1A7 [1A7 [2A2 [2A2 [2A3] 2A4 [OR DI (TOP 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	PAC VIEW) 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32	KAGE V <u>CC</u> 10E 1B1 1B2 1B3 1B4 1B5 1B6 1B7 1B8 1B9 1B10 V <u>CC</u> 2B1 2B2 2B3	
2A3 [2A4 [17	32	2B2 2B3	
2A5 2A6 2A7 2A8 2A8	18 19 20 21 22	31 30 29 28 27	2B4 2B5 2B6 2B7 2B8	
2A10 [GND [23 24	26 25	2B9 2B10	

NC - No internal connection

FUNCTION TABLE (each 10-bit bus switch)

	FUNCTION
L	A port = B port
Н	Disconnect



SCDS068 – JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	\ldots –0.5 V to 7 V
Input voltage range, V _I (see Note 1)	\ldots –0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	l _l = -18 mA				-1.2	V	
		$V_{CC} = 0$	V _I = 5.5 V				10		
'I		V _{CC} = 5.5 V	$V_{I} = 5.5 V \text{ or GND}$				±1	μA	
Icc		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA	
∆lCC [‡]	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA	
Ci	Control inputs	V _I = 3 V or 0						pF	
Cio(OFF)		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF	
ron§		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	l _l = 15 mA					
			V 0	l _l = 64 mA				Ω	
		V _{CC} = 4.5 V	vI=0	I _I = 30 mA					
			V _I = 2.4 V,	lj = 15 mA					

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTPUT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V	
		(0011 01)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
^t en	ŌĒ	A or B					ns
t _{dis}	ŌĒ	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.





SCDS078 - JULY 1998

 25-Ω Switch Connection Between Two Ports 	DGG OR DL PACKAGE (TOP VIEW)
 TTL-Compatible Input Levels Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Shrink Small-Outline (DL) Packages 	NC 1 48 V _{CC} 1A1 2 47 10E 1A2 3 46 1B1 1A3 4 45 1B2
description	1A4 5 44 1B3
The SN74CBTR16861 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.	1A5 6 43 1B4 1A6 7 42 1B5 1A7 8 41 1B6 1A8 9 40 1B7 1A9 10 39 1B8 1A10 11 38 1B9
The device is organized as one dual 10-bit switch with separate output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.	GND [12 37] 1B10 NC [13 36] V _{CC} 2A1 [14 35] 2OE 2A2 [15 34] 2B1 2A3 [16 33] 2B2 2A4 [17 32] 2B3
The device has equivalent $25 \cdot \Omega$ series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.	2A5 [18 31] 2B4 2A6 [19 30] 2B5 2A7 [20 29] 2B6 2A8 [21 28] 2B7
The SN74CBTR16861 is characterized for operation from -40° C to 85°C.	2A9 [22 27] 2B8 2A10 [23 26] 2B9 GND [24 25] 2B10

NC - No internal connection

FUNCTION TABLE (each 10-bit bus switch)

	FUNCTION
L	A port = B port
н	Disconnect

PRODUCT PREVIEW



SCDS078 – JULY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	\ldots –0.5 V to 7 V
Input voltage range, V _I (see Note 1)	\ldots –0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITION	ONS	MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	I _I = -18 mA				-1.2	V	
		$V_{CC} = 0,$	Vj = 5.5 V				10		
'I		V _{CC} = 5.5 V,	V _I = 5.5 V or GND				±1	μΑ	
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			3	μA	
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA	
Ci	Control inputs	V _I = 3 V or 0						pF	
C _{io(OFF)})	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF	
ron§			$V_{\rm b} = 0$	l _l = 64 mA					
		$V_{CC} = 4.5 V$	v] = 0	l _l = 30 mA				Ω	
			$V_1 = 2.4 V_2$	lı = 15 mA					

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A			ns
^t en	ŌĒ	A or B			ns
^t dis	ŌĒ	A or B			ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.





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- DUAL FET BUS SWITCH WITH LEVEL SHIFT SCDS030F - JANUARY 1996 - REVISED MAY 1998 **5-**Ω Switch Connection Between Two Ports D OR PW PACKAGE (TOP VIEW) **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**
- Package Options Include Plastic Small-Outline (D) and Thin Shrink **Small-Outline (PW) Packages**

description

The SN74CBTD3306 features two independent line switches. Each switch is disabled when the associated output-enable (OE) input is high. A diode to V_{CC} is integrated on the chip to allow for level shifting between 5-V inputs and 3.3-V outputs.

1OE

GND Г 4

1A [

1B [3

2

The SN74CBTD3306 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each bus switch) INPUT FUNCTION OE L A port = B port н Disconnect

logic diagram (positive logic)





SN74CBTD3306

] ∨cc 8

20E

5 🛛 2A

7 6 2B

SN74CBTD3306 **DUAL FET BUS SWITCH** WITH LEVEL SHIFTING

SCDS030F - JANUARY 1996 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .	
PW package	
Storage temperature range, T _{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITIONS		MIN	түр‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lı = –18 mA				-1.2	V
VOH		See Figure 2						
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	l _O = 0,	$V_{I} = V_{CC}$ or GND			1.5	mA
∆ICC§	Control inputs	$V_{CC} = 5.5 V,$	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				3		pF
Cio(OFF)		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$			4		pF
			$\lambda = 0$	lj = 64 mA		5	7	
ron¶		V _{CC} = 4.5 V	VI = 0	l _l = 30 mA		5	7	Ω
			$V_{I} = 2.4 V,$	lj = 15 mA		35	50	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

\$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} †	A or B	B or A		0.25	ns
^t en	ŌĒ	A or B	2.1	5.4	ns
^t dis	ŌĒ	A or B	1	4.7	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms





TYPICAL CHARACTERISTICS





- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages



description

The SN74CBTS3306 features independent line switches with Schottky diodes on the I/Os to clamp undershoot. Each switch is disabled when the associated output-enable (\overline{OE}) input is high.

The SN74CBTS3306 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each bus switch)			
INPUT OE FUNCTION			
L	A port = B port		
н	Disconnect		

logic diagram (positive logic)





SN74CBTS3306 **DUAL FET BUS SWITCH** WITH SCHOTTKY DIODE CLAMPING

SCDS029E - JANUARY 1996 - REVISED NOVEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	197°C/W
	PW package	243°C/W
Storage temperature range, T _{stg}		65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	ΜΑΧ	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТĄ	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT
Muz	A or B inputs		h - 19 m A				-0.7	V
VIК	Control inputs	VCC = 4.5 V,	II = -10 IIIA				-1.2	v
	١ _{IL}	V _{CC} = 5.5 V,	V _I = GND				-1	
1	IIН	V _{CC} = 5.5 V,	V _I = 5.5 V				50	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0				5		pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			6		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lı = 15 mA		14	20	
ron¶			$V_{i} = 0$	l _l = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	vi = 0	lı = 30 mA		5	7	
			$V_{ } = 2.4 V,$	lı = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

\$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) pins.



SN74CBTS3306 **DUAL FET BUS SWITCH** WITH SCHOTTKY DIODE CLAMPING SCDS029E - JANUARY 1996 - REVISED NOVEMBER 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		TO	V _{CC} = 4	v	= ۷ _{CC} ± 0.	= 5 V 5 V	UNIT
		(001101)	MIN M	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.35		0.25	ns
ten	ŌĒ	A or B		5.6	1.8	5	ns
t _{dis}	ŌĒ	A or B		4.6	1	4.3	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CI includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tPHL and tPLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING SCDS025K – MAY 1995 – REVISED NOVEMBER 1998

- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Ceramic DIPs (JT), and Ceramic Chip Carriers (FK)

description

The 'CBTD3384 devices provide ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switches allows connections to be made without adding propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting between 5-V inputs and 3.3-V outputs.

These devices are organized as two 5-bit switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN54CBTD3384 is characterized for operation over the full military temperature range from -55° C to 125° C. The SN74CBTD3384 is characterized for operation from -40° C to 85° C.

SN54CBTD3384 JT OR W PACKAGE
SN74CBTD3384 DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

	(,	
10E [1B1 [1A1 [1A2 [1B2 [1B3 [1A3 [1A4 [1B4 [1B5]	1 2 3 4 5 6 7 8 9 10	24 23 22 21 20 19 18 17 16 15	V _{CC} 285 2A5 2A4 284 283 2A3 2A3 2A2 282 282 281
1B5	10	15	2B1
185 [1A5] האס	10 11 12	15 14 13	2B1 2A1 2OF
	12	13	1200

SN54CBTD3384 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

FUNCTION TABLE			
(each 5-bit bus switch)			

INP	UTS	INPUTS/OUTPUTS				
10E	2 <mark>0E</mark>	1B1–1B5	2B1–2B5			
L	L	1A1–1A5	2A1–2A5			
L	Н	1A1–1A5	Z			
Н	L	Z	2A1–2A5			
Н	Н	Z	Z			

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING SCDS025K – MAY 1995 – REVISED NOVEMBER 1998

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		. -0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DBQ package	113°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54CBTD3384		SN74CB1		
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level control input voltage	2		2		V
VIL	Low-level control input voltage		0.8		0.8	V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54CBTD3384, SN74CBTD3384 **10-BIT FET BUS SWITCHES** WITH LEVEL SHIFT ١G

SCDS025K - MAY 1995 - REVISED NOVEMBER 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54CBTD3384			SN74CBTD3384				
		TEST CONDITIONS			MIN	TYP†	MAX	MIN	түр†	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$					-1.2			-1.2	V
VOH		See Figure 2	See Figure 2								
Ц		V _{CC} = 5.5 V,	V _{CC} = 5.5 V, V _I = 5.5 V or GND				±1			±1	μA
ICC		V _{CC} = 5.5 V,	IO = 0,	$V_I = V_{CC} \text{ or } GND$	1.5 1.5			1.5	mA		
∆ICC [‡]	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND					2.5			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				3			3		pF
$C_{io(OFF)}$ $V_O = 3 V \text{ or } 0, \overline{OE} = V_{CC}$				3.5			3.5		pF		
r _{on} §		V _{CC} = 4.5 V	V _I = 0	lı = 64 mA		5			5	7	
				lı = 30 mA		5			5	7	Ω
			V _I = 2.4 V,	lj = 15 mA		35			35	50	

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

	FROM	то	SN54CB1	D3384	SN74CBTD3384		
PARAWETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UNIT
t _{pd} ¶	A or B	B or A		0.25		0.25	ns
ten	ŌĒ	A or B	2.2	9.7	2.3	7	ns
t _{dis}	ŌĒ	A or B	1.5	8.6	1.7	5.3	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

SCDS025K - MAY 1995 - REVISED NOVEMBER 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms





TYPICAL CHARACTERISTICS


SN74CBTS3384 10-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING SCDS024G - MAY 1995 - REVISED MAY 1998

•	Functionally Equivalent to QS3384 and
	QS3L384

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTS3384 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)						
10E	1	24	V _{CC}			
1B1 [2	23	285			
1A1 [3	22	2A5			
1A2 [4	21	2A4			
1B2 [5	20	2B4			
1B3 [6	19	2B3			
1A3 [7	18	2A3			
1A4 [8	17	2A3			
1B4 [9	16	2A2			
1B5 [10	15] 2B1			
1A5 [11	14] 2A1			
CND [12	13] 2 0 E			
	14	10				

The device is organized as two 5-bit bus switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBTS3384 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 5-bit bus switch)						
INPUTS INPUTS/OUTPUTS						
1 <mark>0E</mark>	2 <mark>0E</mark>	1B1–1B5	2B1–2B5			
L	L	1A1–1A5	2A1–2A5			
L	н	1A1–1A5	Z			
н	L	Z	2A1–2A5			
н	Н	Z	Z			



SN74CBTS3384 10-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS024G - MAY 1995 - REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		. $-0.5 \mbox{ V}$ to 7 V
Input voltage range, V _I (see Note 1)		. $-0.3 \; V \; to \; 7 \; V$
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	104°C/W
	DBQ package	113°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}	······································	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN74CBTS3384 **10-BIT FET BUS SWITCH** WITH SCHOTTKY DIODE CLAMPING SCDS024G - MAY 1995 - REVISED MAY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-0.6	V
	۱ _{IL}	V _{CC} = 5.5 V,	VI = GND				-1	
1	IН	V _{CC} = 5.5 V,	V _I = 5.5 V				150	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆lcc‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				6		pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			6.5		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	l _l = 15 mA		14	20	
r _{on} §			V 0	l _l = 64 mA		5	7	Ω
-		V _{CC} = 4.5 V	vI=0	l _l = 30 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		V _{CC} = 4	4 V	= V _{CC} ± 0.	= 5 V 5 V	UNIT
			MIN	МАХ	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.35		0.25	ns
ten	ŌĒ	A or B		6.2	1.9	5.7	ns
^t dis	ŌĒ	A or B		5.5	2.1	5.2	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBTS3384 **10-BIT FET BUS SWITCH** WITH SCHOTTKY DIODE CLAMPING

SCDS024G - MAY 1995 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CI includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.





- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTD3861 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting between 5-V inputs and 3.3-V outputs.

DBQ, DGV, DW, OR PW PACKAGE						
(TOP VIEW)						
L			L			
NC	1	U ₂₄	V _{CC}			
A1 [2	23] OE			
A2 [3	22] B1			
A3 [4	21	B2			
A4 [5	20	B3			
A5 [6	19] B4			
A6 [7	18	B5			
A7 [8	17	B6			
A8 [9	16	B7			
A9 [10	15	B8			
A10[11	14] в9			
GND [12	13	B10			

NC - No internal connection

The device is organized as one 10-bit switch with a single output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

The SN74CBTD3861 is characterized for operation from –40°C to 85°C.

10110	T ON ON ON ONE					
	FUNCTION					
L	A port = B port					
Н	Disconnect					

FUNCTION TABLE

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		0.5 V to 7 V 0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DBQ package	113°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lı = -18 mA				-1.2	V
VOH		See Figure 2						
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC	-	V _{CC} = 5.5 V,	l _O = 0,	$V_I = V_{CC}$ or GND			3	μΑ
⊿ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at $V_{\mbox{CC}}$ or GND			2.5	mA
Ci	Control inputs	$V_I = 3 V \text{ or } 0$						pF
Cio(OFF)		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
			$\lambda t = 0$	lj = 64 mA				
ron¶		$V_{CC} = 4.5 V$	VI = 0	lj = 30 mA				Ω
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



SN74CBTD3861 **10-BIT FET BUS SWITCH** WITH LEVEL SHIFT

SCDS084A - JULY 1998 - REVISED OCTOBER 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
t _{pd} †	A or B	B or A		ns
ten	ŌĒ	A or B		ns
tdis	ŌĒ	A or B		ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms







TYPICAL CHARACTERISTICS

Figure 2. V_{OH} Values



SN74CBTD16210 20-BIT FET BUS SWITCH WITH LEVEL SHIFTING SCDS049C – MARCH 1998 – REVISED MAY 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

The SN74CBTD16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated in the circuit to allow for level shifting between 5-V inputs and 3.3-V outputs.

The device is organized as a dual 10-bit bus switch with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on and A port is connected to B port. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the ports.

The SN74CBTD16210 is characterized for operation from -40° C to 85° C.

DGG, DGV, OR DL PACKAGE								
(TOP VIEW)								
NC [1 U	48] 1 <u>0</u> E					
1A1 [2	47] 2 <u>0E</u>					
1A2 🛛	3	46] 1B1					
1A3 [4	45	1B2					
1A4 [5	44	1B3					
1A5 🛛	6	43] 1B4					
1A6 🛛	7	42] 1B5					
GND [8	41	GND					
1A7 [9	40	1B6					
1A8 [10	39	1B7					
1A9 🛛	11	38	1B8					
1A10	12	37	1B9					
2A1 🛛	13	36	1B10					
2A2 🛛	14	35	2B1					
V _{CC}	15	34	2B2					
2A3 🛛	16	33	2B3					
GND [17	32	GND					
2A4 🛛	18	31	2B4					
2A5 🛛	19	30	2B5					
2A6 🛛	20	29	2B6					
2A7 🛛	21	28	2B7					
2A8 🛛	22	27	2B8					
2A9 🛛	23	26	2B9					
2A10 🛛	24	25	2B10					

NC - No internal connection

FUNCTION TABLE (each 10-bit bus switch)

	FUNCTION		
L	A port = B port		
н	Z		

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN74CBTD16210 20-BIT FET BUS SWITCH WITH LEVEL SHIFTING SCDS049C - MARCH 1998 - REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5	V to 7 V
Input voltage range, V _I (see Note 1)		0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		89°C/W
	DGV package		93°C/W
	DL package		94°C/W
Storage temperature range, T _{stg}		–65°C 1	to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C
-				

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN74CBTD16210 **20-BIT FET BUS SWITCH** WITH LEVEL SHIFTING

SCDS049C - MARCH 1998 - REVISED MAY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER		TEST CONDIT	IONS	MIN	TYP†	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA				-1.2	V
VOH		See Figure 2						
		$V_{CC} = 0 V,$	V _I = 5.5 V				10	
1		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			1.5	mA
∆lcc [‡]	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				4.5		pF
Cio(OFF)		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$			5.5		pF
			$V_{\rm b} = 0$	lj = 64 mA		5	7	
r _{on} §		V _{CC} = 4.5 V	VI = 0	lı = 30 mA		5	7	Ω
			V _I = 2.4 V,	lı = 15 mA		35	50	

[†] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A		0.25	ns
ten	ŌĒ	A or B	1.5	9.8	ns
^t dis	ŌĒ	A or B	1.5	8.9	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBTD16210 **20-BIT FET BUS SWITCH** WITH LEVEL SHIFTING

SCDS049C - MARCH 1998 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





TYPICAL CHARACTERISTICS



SN74CBTD16211 24-BIT FET BUS SWITCH WITH LEVEL SHIFTING SCDS048C – MARCH 1998 – REVISED MAY 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

The SN74CBTD16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated in the circuit to allow for level shifting between 5-V inputs and 3.3-V outputs.

The device is organized as a dual 12-bit bus switch with separate output-enable (\overline{OE}) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is on and A port is connected to B port. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the ports.

The SN74CBTD16211 is characterized for operation from -40° C to 85° C.

DGG, DGV, OR DL PACKAGE							
лс Г		56					
1A1 [2	55					
1A2	3	54	1 1 1 1 1 1 1 1 1 1 1 1 1 1				
1A3 [4	53	1B2				
1A4 [5	52	1B3				
1A5 🛛	6	51	1B4				
1A6	7	50	1B5				
GND	8	49	GND				
1A7 🛛	9	48	1B6				
1A8 [10	47]1B7				
1A9 🛛	11	46]1B8				
1A10 🛛	12	45]1B9				
1A11 [13	44]1B10				
1A12 🛛	14	43]1B11				
2A1 🛛	15	42]1B12				
2A2 🛛	16	41]2B1				
V _{CC} [17	40]2B2				
2A3 [18	39]2B3				
GND [19	38] GND				
2A4 [20	37	2B4				
2A5 [21	36	2B5				
2A6 [22	35	2B6				
2A7 [23	34	2B7				
2A8 _	24	33	2B8				
2A9 [25	32	2B9				
2A10	26	31	2B10				
2A11 [27	30	2B11				
2A12	28	29	2B12				

NC - No internal connection

FUNCTION TABLE (each 12-bit bus switch)

	FUNCTION
L	A port = B port
Н	Disconnect



SN74CBTD16211 24-BIT FET BUS SWITCH WITH LEVEL SHIFTING SCDS048C - MARCH 1998 - REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	V to 7 V $\!\!\!\!$
Input voltage range, V _I (see Note 1)		-0.5	V to 7 V $\!\!\!$
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		65°C f	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТĄ	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
VOH		See Figure 2						
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			1.5	mA
$\Delta I C C^{\ddagger}$	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				3		pF
Cio(OFF)		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$			5.5		pF
			$\lambda = 0$	lı = 64 mA		5	7	
r _{on} §		$V_{CC} = 4.5 V$	VI = 0	lı = 30 mA		5	7	Ω
			V _I = 2.4 V,	lj = 15 mA		35	50	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
tpd¶	A or B	B or A		0.25	ns
ten	ŌĒ	A or B	1.5	9.8	ns
^t dis	ŌĒ	A or B	1.5	8.9	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBTD16211 24-BIT FET BUS SWITCH WITH LEVEL SHIFTING

SCDS048C - MARCH 1998 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tPLZ and tPHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





TYPICAL CHARACTERISTICS



SN74CBTS16211 24-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING SCDS050B – MARCH 1998 – REVISED MAY 1998

- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

The SN74CBTS16211 provides 24 bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can operate as a dual 12-bit bus switch or a single 24-bit bus switch. When $1\overline{OE}$ is low, 1A is connected to 1B. When $2\overline{OE}$ is low, 2A is connected to 2B.

The SN74CBTS16211 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE (each 12-bit bus switch)

	FUNCTION
L	A port = B port
н	Disconnect

DGG, DG	V, OR D (TOP VI	EW)					
NC [$_{1}$ U	56] 1 <u>0</u> E				
1A1 [2	55	20E				
1A2 🛛	3	54]1B1				
1A3 🛛	4	53]1B2				
1A4 [5	52]1B3				
1A5 🛛	6	51]1B4				
1A6 🛛	7	50] 1B5				
GND 🛛	8	49] GND				
1A7 [9	48]1B6				
1A8	10	47] 1B7				
1A9	11	46] 1B8				
1A10	12	45	1B9				
1A11	13	44]1B10				
1A12	14	43] 1B11				
2A1 🛛	15	42]1B12				
2A2	16	41	2B1				
V _{CC}	17	40	2B2				
2A3 🛛	18	39] 2B3				
GND 🛛	19	38] GND				
2A4 🛛	20	37	2B4				
2A5 🛛	21	36	2B5				
2A6	22	35	2B6				
2A7 🛛	23	34] 2B7				
2A8 🛛	24	33] 2B8				
2A9 🛛	25	32	2B9				
2A10 🛛	26	31	2B10				
2A11 🛛	27	30	2B11				
2A12 🛛	28	29	2B12				

NC - No internal connection



SN74CBTS16211 24-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING SCDS050B – MARCH 1998 – REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	V to 7 V $\!\!\!\!$
Input voltage range, V _I (see Note 1)		-0.5	V to 7 V $\!\!\!$
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		65°C f	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
ТĄ	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN74CBTS16211 24-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING SCDS050B – MARCH 1998 – REVISED MAY 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITION	ONS	MIN	TYP†	MAX	UNIT
۷IK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
	Ι _{ΙL}	V _{CC} = 5.5 V,	VI = GND				-1	
1	ЧΗ	V _{CC} = 5.5 V,	V _I = 5.5 V				150	μA
ICC		V _{CC} = 5.5 V,	l _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆lCC‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	$V_{I} = 3 V \text{ or } 0$				3		pF
C _{io(OFF)})	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			5.5		pF
		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		14	20	
_{ron} §			$\lambda = 0$	lj = 64 mA		5	7	Ω
		V _{CC} = 4.5 V	vI=0	lı = 30 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		8	12	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		TO	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT	
			MIN	MAX	MIN	MAX		
t _{pd} ¶	A or B	B or A		0.35		0.25	ns	
t _{en}	ŌĒ	A or B		9.3	3.3	8.6	ns	
^t dis	ŌĒ	A or B		7.1	2.8	7.9	ns	

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SN74CBTS16211 24-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS050B - MARCH 1998 - REVISED MAY 1998



PARAMETER MEASUREMENT INFORMATION

NOTES: A. CI includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SN74CBTS16212 24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPING SCDS036B – DECEMBER 1997 – REVISED MAY 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTS16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN74CBTS16212 is characterized for operation from -40° C to 85° C.

DGG, DG	V, OR D	L P	ACKAGE
	(TOP VI	EW))
4			L
S0 L	1	56	LS1
1A1 L	2	55	S2
1A2 🛛	3	54	1B1
2A1 L	4	53	1B2
2A2 🛛	5	52	2B1
3A1 🛛	6	51	2B2
3A2 🛛	7	50	3B1
GND [8	49	GND
4A1 🛛	9	48	3B2
4A2 🛛	10	47	4B1
5A1 🛛	11	46	4B2
5A2 🛛	12	45	5B1
6A1 [13	44	5B2
6A2 🛛	14	43	6B1
7A1 🛛	15	42	6B2
7A2 🛛	16	41	7B1
V _{CC}	17	40	7B2
8A1 🛛	18	39	8B1
GND [19	38	GND
8A2 🛛	20	37	8B2
9A1 🛛	21	36	9B1
9A2 🛛	22	35	9B2
10A1 🛛	23	34	10B1
10A2 🛛	24	33	10B2
11A1 🛛	25	32	11B1
11A2 🛛	26	31	11B2
12A1 🛛	27	30	12B1
12A2 🛛	28	29	12B2

INPUTS			INPUTS/	OUTPUTS	FUNCTION		
S2	S 1	S0	A1	A2	FUNCTION		
L	L	L	Z	Z	Disconnect		
L	L	Н	B1	Z	A1 port = B1 port		
L	н	L	B2	Z	A1 port = B2 port		
L	н	н	Z	B1	A2 port = B1 port		
н	L	L	Z	B2	A2 port = B2 port		
н	L	н	Z	Z	Disconnect		
н	Н	L	B1	B2	A1 port = B1 port A2 port = B2 port		
Н	Н	Н	B2	B1	A1 port = B2 port A2 port = B1 port		

ELINCTION TABLE

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74CBTS16212 24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPING SCDS036B – DECEMBER 1997 – REVISED MAY 1998

logic diagram (positive logic)





SN74CBTS16212 24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMP

SCDS036B - DECEMBER 1997 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5	V to 7 V
Input voltage range, V _I (see Note 1)		-0.5	V to 7 V
Continuous channel current			128 mA
Input clamp current, I_{IK} (V _I < 0)			–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		81°C/W
	DGV package		86°C/W
	DL package		74°C/W
Storage temperature range, T _{stg}		₀5°C t	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

5.5	V
	V
0.8	V
85	°C
-	0.8 85

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITION	ONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = -18 mA				-1.2	V
	۱ _{IL}	V _{CC} = 5.5 V,	V _I = GND				-1	
Ч 	IIН	V _{CC} = 5.5 V,	V _I = 5.5 V				150	μΑ
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μA
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0				2.5		pF
Cio(OFF)		V _O = 3 V or 0,	S0, S1, or S2 = V _{CC}	;		10.5		pF
		$V_{CC} = 4 V,$	V _I = 2.4 V,	lj = 15 mA			20	
r _{on} ¶			$\lambda = 0$	lj = 64 mA		4	7	0
		V _{CC} = 4.5 V	v] = 0	lı = 30 mA		4	7	52
		V	V _I = 2.4 V,	lj = 15 mA		6	12	

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBTS16212 24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS036B - DECEMBER 1997 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER			V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.35		0.25	ns
^t pd	S	A or B		10	1.5	9.1	ns
t _{en}	S	A or B		10.4	1.5	9.7	ns
^t dis	S	A or B		9.2	1.5	8.8	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CI includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTS16213 provides 24 bits of high-speed TTL-compatible bus switching or exchanging with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN74CBTS16213 is characterized for operation from -40° C to 85° C.

DGG OR DL PACKAGE (TOP VIEW)						
			,			
sol	1	\bigcirc 56	s	1		
1A1 🛛	2	55] s:	2		
1A2	3	54	16	31		
2A1	4	53	16	32		
2A2	5	52	28	B1		
3A1	6	51	28	32		
3A2	7	50] 3E	31		
GND	8	49] G	ND		
4A1	9	48] 3E	32		
4A2	10	47] 48	31		
5A1	11	46] 48	32		
5A2	12	45	5	31		
6A1	13	44] 5E	32		
6A2	14	43] 6E	31		
7A1	15	42] 6E	32		
7A2	16	41] 78	31		
V _{CC}	17	40	76	32		
8A1	18	39	88	31		
GND	19	38] G	ND		
8A2	20	37	88	32		
9A1	21	36	0 9E	31		
9A2	22	35	98	32		
10A1	23	34] 1()B1		
10A2	24	33] 1()B2		
11A1	25	32] 11	B1		
11A2	26	31	[] 11	B2		
12A1	27	30] 12	2B1		
12A2	28	29] 12	2B2		

	INPUTS		INPUTS/OUTPUTS		EUNCTION
S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	Н	B1 port	Z	A1 port = B1 port
L	Н	L	B2 port	Z	A1 port = B2 port
L	н	Н	Z	B1 port	A2 port = B1 port
Н	L	L	Z	B2 port	A2 port = B2 port
н	L	Н	Z	Z	Disconnect
Н	Н	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
н	Н	Н	B2 port	B1 port	A1 port = B2 port A2 port = B1 port

FUNCTION TABLE



SN74CBTS16213 24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPING SCDS051A – MARCH 1998 – REVISED MAY 1998

logic diagram (positive logic)





SN74CBTS16213 24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPIN

SCDS051A - MARCH 1998 - REVISED MAY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		V to 7 V
Input voltage range, V _I (see Note 1)		V to 7 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	81°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	typ‡	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
1.	۱ _{IL}	V _{CC} = 5.5 V,	V _I = GND				-1	
1	Ιн	V _{CC} = 5.5 V,	V _I = 5.5 V				50	μА
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μΑ
∆ICC§	Control inputs	$V_{CC} = 5.5 V,$	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				4.5		рF
	B port	$V_{a} = 2 V_{ar} 0$	S0, S1, or S2 = V_{CC}			8.5		ъĘ
Cio(OFF)	A port	$v_{O} = 3 v \text{ or } 0,$				8		рг
	A to B or B to A	$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		14	20	
		A to B or B to A $V_{CC} = 4.5 V$	V _I = 0	lj = 64 mA		5	7	
				lı = 30 mA		5	7]
			V _I = 2.4 V,	lj = 15 mA		8	15	0
^r on ^{II}		$V_{CC} = 4 V,$ TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lj = 15 mA		22	30	52
	A1 to A2		$V_{t} = 0$	lj = 64 mA		10	14	
		V _{CC} = 4.5 V	v] = 0	lı = 30 mA		10	14	
		V _I = 2.4	V _I = 2.4 V,	lj = 15 mA		16	22	

[‡] All typical values are at $V_{CC} = 5 V$ (unless otherwise noted), $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBTS16213 24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS051A - MARCH 1998 - REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTPUT)	V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT	
	(INFOT)	(0011 01)	MIN MAX	MIN	MAX		
+	A or B	B or A	0.35		0.25		
^t pd ¹	A1	A2	0.5		0.5	ns	
t _{en}	S	A or B	12.4	3.2	11.1	ns	
^t dis	S	A or B	12.4	2.3	11.9	ns	
t _{en}	S0	A2 and B2	11.5	4	10.9	ns	
^t dis	S0	A2 and B2	12.8	5.7	12	ns	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.





- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Shrink Small-Outline (DL) Packages

description

The SN74CBTD16861 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting between 5-V inputs and 3.3-V outputs.

The device is organized as one dual 10-bit switch with separate output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

The SN74CBTD16861 is characterized for operation from -40° C to 85° C.

DGG OR DL PACKAGE (TOP VIEW)						
NC [1A1 [1A2 [1A3 [1A4 [1A5] 1A6 [1 2 3 4 5 6 7	48 47 46 45 44 43 42	V <u>CC</u> 10E 181 182 183 184 185			
1A7 [8 0	41 40] 1B6			
1A9 [9 10 11	40 39 20	1B7 1B8			
GND	12	30 37	1B9 1B10			
NC L 2A1 [13 14	36 35	V _{CC} 20E			
2A2 [15	34	2B1			
2A3 L	16	33	2B2			
2A4 L	17	32] 2B3] 2B3			
2A5 L 246 [10	30	1 285			
2A7	20	29	2B6			
2A8	21	28	2B7			
2A9 🛛	22	27	2B8			
2A10	23	26	2B9			
GND [24	25	2B10			

NC - No internal connection

FUNCTION TABLE (each 10-bit bus switch)

	FUNCTION
L	A port = B port
Н	Disconnect



SN74CBTD16861 20-BIT FET BUS SWITCH WITH LEVEL SHIFTING SCDS069B – JULY 1998 – REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Package thermal impedance, θ_{JA} (see Note 2): DGG package	
DL package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN74CBTD16861 20-BIT FET BUS SWITCH WITH LEVEL SHIFTING

SCDS069B - JULY 1998 - REVISED OCTOBER 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	түр†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	V
VOH		See Figure 2						
Ц		V _{CC} = 5.5 V,	$V_I = 5.5 V \text{ or GND}$				±1	μA
ICC		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			1.5	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	VI = 3 V or 0						pF
C _{io(OFF})	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
			$V_{\rm H} = 0$	lj = 64 mA				
r _{on} §		$V_{CC} = 4.5 V$	v] = 0	lı = 30 mA				Ω
			$V_1 = 2.4 V_1$	lı = 15 mA				

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	МАХ	UNIT
t _{pd} ¶	A or B	B or A			ns
^t en	ŌE	A or B			ns
^t dis	ŌĒ	A or B			ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).





PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns. t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.











General Information	
CBT Single Gates	
CBT (2 to 10 Bit)	
CBT Widebus™	
CBT With Integrated Diodes	
CBTLV Single Gates	
CBTLV (2 to 10 Bit)	
CBTLV Widebus™	
Application Reports	
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DBV PACKAGE (TOP VIEW)

5 V_{CC}

4 B

OE

GND 13

A 🛛 2

SCDS057B - MARCH 1998 - REVISED OCTOBER 1998

- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Packaged in Plastic Small-Outline Transistor Package

description

The SN74CBTLV1G125 features a single high-speed line switch. The switch is disabled when the output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV1G125 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE					
	FUNCTION				
L	A port = B port				
Н	Disconnect				

logic diagram (positive logic)



simplified schematic, each FET switch



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2)	347°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
VIH	V _{CC} = 2.3 V to	2.7 V	1.7		V
	Note that the second of the second of the second s		2		v
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			0.7	V
VIL	V _{CC} = 2.7 V to	3.6 V		0.8	v
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT	
VIK		V _{CC} = 3 V,	lj = -18 mA				-1.2	V
lj		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±1	μΑ
loff		$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 3.6 \text{ V}$	1			10	μΑ
ICC	_	V _{CC} = 3.6 V,	I _O = 0,	$V_{I} = V_{CC}$ or GND			10	μΑ
∆ICC§	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	VI = 3 V or 0						pF
C _{io(OFF}	F)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
			$\lambda = 0$	lı = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	VI = 0	lı = 24 mA				
r ¶			V _I = 1.7 V,	lı = 15 mA				0
'on "			$V_{1} = 0$	l _l = 64 mA				52
		$V_{CC} = 3 V$	VI = 0	l _l = 24 mA				
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SCDS057B - MARCH 1998 - REVISED OCTOBER 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPLIT)	TO (OUTPUT)	V _{CC} = 2.5 V V _{CC} = 3.3 ± 0.2 V ± 0.3 V		3.3 V 3 V	UNIT	
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A					ns
ten	ŌĒ	A or B					ns
^t dis	ŌĒ	A or B					ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl $_{7}$ and tpH $_{7}$ are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .





PRODUCT PREVIEW

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NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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SCDS037C - DECEMBER 1997 - REVISED OCTOBER 1998

- Standard '125-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTLV3125 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (\overline{OE}) input is high.

D, DGV,	OF (TO	r PW P VII	PA EW)	CKAGE
10E 1A 1B 20E 2A 2B	1 2 3 4 5 6	υ	14 13 12 11 10 9	V _{CC} 4OE 4A 4B 3OE 3A
GND [7		8] 3B

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3125 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each bus switch)				
INPUT OE FUNCTION				
L	A port = B port			
Н	Disconnect			

logic diagram (positive logic)





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SCDS037C - DECEMBER 1997 - REVISED OCTOBER 1998

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: D package	127°C/W
	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
VIH	High lovel control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
	$V_{CC} = 2.7 \text{ V to } 3.$	V_{CC} = 2.7 V to 3.6 V	2		v
VIL	Low level central input veltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	Notice the set of the			0.8	v
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITION	ONS	MIN	түр†	MAX	UNIT
VIK		V _{CC} = 3 V,	l _l = –18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_{I} = V_{CC} \text{ or } GND$				±5	μA
loff		$V_{CC} = 0,$	V_{I} or $V_{O}=0$ to 4.5 \	1			10	μA
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			10	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	VI = 3 V or 0						pF
C _{io(OFI}	F)	V _O = 3 V or 0,	$\overline{OE} = VCC$					pF
			N/4 0	lı = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	VI = 0	lı = 24 mA				
r _{on} §			V _I = 1.7 V,	l _l = 15 mA				0
			Nr. 0	II = 64 mA				52
		$V_{CC} = 3 V$	v] = 0	lı = 24 mA				
			V _I = 2.4 V,	lj = 15 mA				

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		(001201)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
ten	ŌĒ	A or B					ns
tdis	ŌĒ	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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NOTES: A. CI includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tPLZ and tPHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS037C - DECEMBER 1997 - REVISED OCTOBER 1998



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms



SCDS038C - DECEMBER 1997 - REVISED OCTOBER 1998

- Standard '126-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

D, DGV, OR PW PACKAGE (TOP VIEW)							
	4	U,	ከ./				
	1	14	F vcc				
1A L	2	13	40E				
1B [3	12] 4A				
20E [4	11] 4B				
2A 🛛	5	10] 30E				
2B 🛛	6	9] 3A				
GND [7	8] зв				
	-						

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3126 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each bus switch)			
INPUT OE	FUNCTION		
L	Disconnect		
н	A port = B port		

logic diagram (positive logic)





PRODUCT PREVIEW

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SCDS038C - DECEMBER 1997 - REVISED OCTOBER 1998

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	0).5 V to 4.6 V
Input voltage range, V _I (see Note 1)	().5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	127°C/W
	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{stg}		5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
Viu High lovel control input voltage		V_{CC} = 2.3 V to 2.7 V	1.7		V
VН	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		v	
	Low-level control input voltage $V_{CC} = 2.3 \vee to 2.7 \vee$ $V_{CC} = 2.7 \vee to 3.6 \vee$			0.7	v
۷IL				0.8	
T _A Operating free-air temperature		-40	85	°C	

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCDS038C - DECEMBER 1997 - REVISED OCTOBER 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITION	ONS	MIN	түр†	MAX	UNIT
VIK		V _{CC} = 3 V,	l _l = –18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_{I} = V_{CC} \text{ or } GND$				±5	μA
loff		$V_{CC} = 0,$	V_{I} or $V_{O}=0$ to 4.5 \	1			10	μA
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			10	μA
ΔI_{CC}^{\ddagger}	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{io(OFf}	F)	V _O = 3 V or 0,	OE = VCC					pF
				lı = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at Vcc = 2.5 V	$V_{I} = 0$	lı = 24 mA				
r _{on} §			V _I = 1.7 V,	l _l = 15 mA				0
			Nr. 0	II = 64 mA				52
		$V_{CC} = 3 V$	v] = 0	lı = 24 mA				
			V _I = 2.4 V,	l _l = 15 mA				

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
ten	OE	A or B					ns
^t dis	OE	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



SCDS038C - DECEMBER 1997 - REVISED OCTOBER 1998



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SCDS038C - DECEMBER 1997 - REVISED OCTOBER 1998



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns. D. The outputs are measured one at a time with one transition per measurement.
- D. The outputs are measured one at a tin
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



SCDS034G - JULY 1997 - REVISED SEPTEMBER 1998

 Standard '245-Type Pinout 5-Ω Switch Connection Between Two Ports 	DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)
Isolation Under Power-Off Conditions	
 ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	A1 [2 19] OE A2 [3 18] B1 A3 [4 17] B2
 Latch-Up Performance Exceeds 250 mA Per JESD 17 	A4 [5 16] B3 A5 [6 15] B4
 Package Options Include Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages 	A6 [7 14] B5 A7 [8 13] B6 A8 [9 12] B7 GND [10 11] B8
raukayes	NC – No internal connection

description

The SN74CBTLV3245A provides eight bits of high-speed bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When output enable (\overline{OE}) is low, the 8-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3245A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE				
	FUNCTION			
L	A port = B port			
Н	Disconnect			

logic diagram (positive logic)





SCDS034G - JULY 1997 - REVISED SEPTEMBER 1998

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		-0.5 V to 4.6 V
Continuous shannel surrent		. 0.0 V t0 4.0 V
	• • • • • • • • • • • • • • • • • • • •	120 IIIA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		
Package thermal impedance, θ_{JA} (see Note 2):	: DBQ package	113°C/W
	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC} Supply voltage			3.6	V
	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIН	Sign-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		v
M.	Low-level control input voltage $\frac{V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}}{V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}}$		0.7	V
۷IL			0.8	↓ v
T _A Operating free-air temperature			85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
Muz	Control inputs	$\lambda = 2 \lambda$	lı_ 19 m∆	· _ 19 m /			-1.2	V
۷IK	Data inputs	VCC = 3 V,	η = -10 ΠΑ				-0.8	v
Ц		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±60	μΑ
loff		V _{CC} = 0,	$V_{I} \text{ or } V_{O} = 0 \text{ to } 3.6 \text{ V}$				40	μΑ
ICC		V _{CC} = 3.6 V,	l _O = 0,	$V_{I} = V_{CC}$ or GND			20	μΑ
∆lcc‡	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μΑ
Ci	Control inputs	V _I = 3 V or 0				4		pF
C _{io(OFF}	=)	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$			9		pF
		$V_{CC} = 2.3 V,$	V _I = 0	I _O = 64 mA		5	8	
				I _O = 24 mA		5	8	
r _{on} §		111 41 100 - 2.0 1	V _I = 1.7 V,	l _O = 15 mA		27	40	0
			$\lambda = 0$	I _O = 64 mA		5	7	52
		$V_{CC} = 3 V$	V] = 0	I _O = 24 mA		5	7	
			$V_{ } = 2.4 V_{,}$	I _O = 15 mA		10	15	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO	V _{CC} = ± 0.2	2.5 V 2 V	= ۷ _{CC} ± 0.3	3.3 V 3 V	UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.15		0.25	ns
^t en	ŌĒ	A or B	1	6	1	4.7	ns
^t dis	ŌĒ	A or B	1	6.1	1	6.4	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).



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NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tPZL and tPZH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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NOTES: A. $C_{\mbox{L}}$ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 0 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tp_I H and tp_{HI} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms



- Functionally Equivalent to QS3251
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTLV3251 device is a 1-of-8 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

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DGV, DW, OR PW PACKAGE (TOP VIEW)							
В4 [В3 [16	V _{CC} B5				
B2 []	3 [,] 1 [,]	14 13	B6 B7				
	5 ⁴		B8 S0				
	o 7 [,]		S0 S1				
	D	۶H	32				

NC - No internal connection

The select inputs (S0, S1, S2) control the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3251 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE								
INPUTS				EUNCTION				
OE	S2	S 1	S0	FUNCTION				
L	L	L	L	A port = B1 port				
L	L	L	Н	A port = B2 port				
L	L	Н	L	A port = B3 port				
L	L	Н	Н	A port = B4 port				
L	н	L	L	A port = B5 port				
L	н	L	Н	A port = B6 port				
L	н	н	L	A port = B7 port				
L	н	Н	Н	A port = B8 port				
н	Х	Х	Х	Disconnect				

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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logic diagram (positive logic)



simplified schematic, each FET switch





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{K} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGV package	180°C/W
	DW package	105°C/W
	PW package	149°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

⁺ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC} Supply voltage			2.3	3.6	V
VIH	High lovel control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
	High-level control linput voltage	V_{CC} = 2.7 V to 3.6 V	2		v
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			0.7	V
VIL	Low-level control linput voltage	V_{CC} = 2.7 V to 3.6 V		0.8	v
T _A Operating free-air temperature			-40	85	°C
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ Operating free-air temperature		-40		0.8 85

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	түр‡	MAX	UNIT	
VIK		V _{CC} = 3 V,	l _l = –18 mA				-1.2	V	
lj		V _{CC} = 3.6 V,	$V_{I} = V_{CC} \text{ or } GND$				±1	μA	
loff		$V_{CC} = 0,$	V_{I} or $V_{O} = 0$ to 4.5	5 V			10	μA	
ICC		V _{CC} = 3.6 V,	$I_{O} = 0,$ $V_{I} = V_{CC} \text{ or } GND$				10	μA	
∆ICC§	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA	
Ci	Control inputs	VI = 3 V or 0						pF	
0	A port		$\overline{OE} = V_{CC}$					~ Г	
Cio(OFF)	B port	vO = 3 v or 0,						рг	
			\/ ₀	lj = 64 mA					
		$V_{CC} = 2.3 V,$	V = 0	lj = 24 mA					
r _{on} ¶			V _I = 1.7 V,	lj = 15 mA				0	
				lj = 64 mA				52	
		$V_{CC} = 3 V$	V] = 0	lj = 24 mA				1	
			VI = 2.4 V,	lj = 15 mA					

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
		(001101)	MIN	MAX	MIN	MAX		
	A or B [†]	B or A						
^t pd	S	А					ns	
t _{en}	S	В					ns	
^t dis	S	В					ns	
t _{en}	ŌĒ	A or B					ns	
^t dis	ŌE	A or B					ns	

[†] The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Ω = 50 Ω, t_f ≤ 2 ns, t_f ≤ 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .





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NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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- Functionally Equivalent to QS3253
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTLV3253 is a dual 1-of-4 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

DGV, DW, OR PW PACKAGE (TOP VIEW)							
10E	1	16] V _{CC}				
S1	2	15] 2OE				
1B4	3	14] S0				
1B3	4	13] 2B4				
1B2	5	12] 2B3				
1B1	6	11] 2B2				
1A	7	10] 2B1				
GND	8	9] 2A				

The select (S0, S1) inputs control the data flow. The FET multiplexers/demultiplexers are disabled when the associated output-enable $\overline{(OE)}$ input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3253 is characterized for operation from -40°C to 85°C.

(each multiplexer/demultiplexer)							
	INPUTS		EUNCTION				
OE	S1	S0	FUNCTION				
L	L	L	A port = B1 port				
L	L	Н	A port = B2 port				
L	н	L	A port = B3 port				
L	Н	Н	A port = B4 port				
н	Х	Х	Disconnect				

FUNCTION TABLE



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logic diagram (positive logic)



simplified schematic, each FET switch





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range. Vcc		. –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGV package	180°C/W
	DW package	105°C/W
	PW package	149°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC} Supply voltage			2.3	3.6	V
VIH	High level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
	High-level control linput voltage	V_{CC} = 2.7 V to 3.6 V	2		v
VIL	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			0.7	V
	Low-level control linput voltage	V_{CC} = 2.7 V to 3.6 V		0.8	v
TA	Operating free-air temperature		-40	85	°C
V _{IL} T _A	Low-level control input voltage Operating free-air temperature	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		-40	0.7 0.8 -40 85

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			түр‡	MAX	UNIT
VIK	V_{IK} $V_{CC} = 3 V$, $I_I = -18 mA$				-1.2	V		
Ц		V _{CC} = 3.6 V,	$V_{I} = V_{CC}$ or GND				±1	μA
loff		$V_{CC} = 0,$	V_{I} or $V_{O}=0$ to 4.5	V			10	μA
ICC		V _{CC} = 3.6 V,	IO = 0,	$V_I = V_{CC}$ or GND			10	μA
∆ICC§	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	VI = 3 V or 0						pF
0	A port		$\overline{OE} = V_{CC}$					۶E
	B port	$v_{O} = 3 v \text{ or } 0,$						рг
			$\lambda = 0$	lj = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	VI = 0	lj = 24 mA				
r _{on} ¶			V _I = 1.7 V,	l _l = 15 mA				0
			$\lambda = 0$	lj = 64 mA				52
		$V_{CC} = 3 V$	VI = 0	lj = 24 mA				
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		(001701)	MIN	MAX	MIN	MAX	
^t pd	A or B†	B or A					20
	S	A or B					115
t _{en}	S	A or B					ns
^t dis	S	A or B					ns
t _{en}	ŌĒ	A or B					ns
^t dis	ŌĒ	A or B					ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2 ns, t_f ≤ 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.





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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



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- Functionally Equivalent to QS3257
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTLV3257 is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

DGV, DW, OR PW PACKAGE (TOP VIEW)								
S [1B1 [1B2 [1A [2B1 [2B2 [2A [GND [1 2 3 4 5 6 7 8	16 15 14 13 12 11 10 9	V _{CC} OE 4B1 4B2 4A 3B1 3B2 3A					

The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3257 is characterized for operation from -40°C to 85°C.

INP	JTS	EUNCTION						
OE S		FUNCTION						
L	L	A port = B1 port						
L	Н	A port = B2 port						
н	Х	Disconnect						

FUNCTION TABLE



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logic diagram (positive logic)



PRODUCT PREVIEW

simplified schematic, each FET switch





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		. –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGV package	180°C/W
	DW package	105°C/W
	PW package	149°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

⁺ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
V _{CC} Supply voltage			2.3	3.6	V	
	High lovel control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V	
I [∨] IH	High-level control input voltage	V_{CC} = 2.7 V to 3.6 V	2		v	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
VIL	Low-level control linput voltage	V_{CC} = 2.7 V to 3.6 V		0.8	v	
T _A Operating free-air temperature			-40	85	°C	
	Operating free-air temperature	$V_{CC} = 2.7 V \text{ to } 3.6 V$	-40		0.8 85	

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			TYP‡	MAX	UNIT
VIK		V _{CC} = 3 V,	l _l = –18 mA	I _I = -18 mA			-1.2	V
Ц		V _{CC} = 3.6 V,	V _I = V _{CC} or GND				±1	μA
l _{off}		$V_{CC} = 0,$	V_{I} or $V_{O}=0$ to 4.5 V				10	μA
Icc		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆ICC§	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0						pF
	A port		$\overline{OE} = V_{CC}$					۶E
	B port	$v_{O} = 3 v \text{ or } 0,$						рг
			$I_I = 64 \text{ mA}$					
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	VI=0	lı = 24 mA				
r _{on} ¶		111 41 100 - 2.0 1	V _I = 1.7 V,	l _l = 15 mA				0
			V/ 0	lı = 64 mA				52
		$V_{CC} = 3 V$	VI = 0	lı = 24 mA				
			$V_{I} = 2.4 V,$	lj = 15 mA				

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
	(INFOT)	(001701)	MIN	MAX	MIN	MAX		
^t pd	A or B†	B or A						
	S	A or B					ns	
t _{en}	S	A or B					ns	
^t dis	S	A or B					ns	
ten	ŌE	A or B					ns	
^t dis	OE	A or B					ns	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2 ns, t_f ≤ 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.




SN74CBTLV3257 LOW-VOLTAGE 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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PARAMETER MEASUREMENT INFORMATION

NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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•	Functionally Equivalent to QS3383 and QS3L383	DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)					
•	5- Ω Switch Connection Between Two Ports						
•	Isolation Under Power-Off Conditions	1B1 2 23 5B2					
•	ESD Protection Exceeds 2000 V Per	1A1 [] 3 22] 5A2					
	MIL-STD-883, Method 3015; Exceeds 200 V						
	Using Machine Model (C = 200 pF, R = 0)	1B2 5 20 5B1					
•	Latch-Up Performance Exceeds 250 mA Per	2B1 6 19 4B2					
	JESD 17						
•	Package Options Include Shrink						
	Small-Outline (DBQ), Thin Verv	2B2 U 9 16 U 4B1					
	Small-Outline (DGV), Small-Outline (DW).	3B1 10 15 3B2					
	and Thin Shrink Small-Outline (PW)	3A1 U 11 14 U 3A2					
	Packages	GND L 12 13 BX					

description

The SN74CBTLV3383 provides ten bits of high-speed bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high and BE is low.

The SN74CBTLV3383 is characterized for operation from -40°C to 85°C.

INP	UTS	INPUTS/OUTPUTS			
BE	ΒХ	1A1–5A1	1A2–5A2		
L	L	1B1–5B1	1B2–5B2		
L	н	1B2–5B2	1B1–5B1		
Н	Х	Z	Z		

FUNCTION TABLE



SCDS047C - MARCH 1998 - REVISED NOVEMBER 1998

logic diagram (positive logic)



simplified schematic, each FET switch





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V 0.5 V to 4.6 V
		120 MA
Input clamp current, I_{IK} ($v_{I/O} < 0$)		–50 MA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	103°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
VIH	High lovel control input veltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
	High-lever control input voltage	$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		v
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			0.7	V
۷IL	Low-level control input voltage	$V_{CC} = 2.7 V \text{ to } 3.6 V$		0.8	v
Т _А	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 3 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±1	μA
l _{off}		$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 3.6 \text{ V}$				10	μA
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_{I} = V_{CC}$ or GND			10	μA
∆lCC§	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0				3.5		pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{BE} = V_{CC}$			13.5		pF
		$V_{CC} = 2.3 V,$	V. – 0	lı = 64 mA		5	8	
			V] = 0	lı = 24 mA		5	8	
r _{on} ¶			V _I = 1.7 V,	lj = 15 mA		27	40	0
			$V_{\rm b} = 0$	l _l = 64 mA		5	7	52
		$V_{CC} = 3 V$	V] = 0	lj = 24 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER			V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		(001201)	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.15		0.25	ns
^t pd	BX	A or B	1.5	5.8	1.5	4.7	ns
t _{en}	BE	A or B	1.5	5.3	1.5	4.7	ns
^t dis	BE	A or B	1	6	1	6	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2 ns, t_f ≤ 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- D. The outputs are measured one at a time with one tra
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS047C - MARCH 1998 - REVISED NOVEMBER 1998



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



SCDS059B - MARCH 1998 - REVISED SEPTEMBER 1998

 Functionally Equivalent to QS3384 and QS3L384 	DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)				
 5-Ω Switch Connection Between Two Ports 					
 Isolation Under Power-Off Conditions 	1B1 2 23 2B5				
ESD Protection Exceeds 2000 V Per	1A1 🛛 3 22 🕽 2A5				
MIL-STD-883, Method 3015; Exceeds 200 V	1A2 🛛 4 21 🗋 2A4				
Using Machine Model (C = 200 pF, R = 0)	1B2 🛛 5 20 🗋 2B4				
Latch-Up Performance Exceeds 250 mA Per	1B3 🛛 6 19 🗋 2B3				
JESD 17	1A3 [7 18 [2A3				
Package Options Include Shrink	1A4 🛛 8 17 🗋 2A2				
Small-Outline (DBQ). Thin Verv	1B4 U 9 16 2B2				
Small-Outline (DGV), Small-Outline (DW).	1B5 U 10 15 2B1				
and Thin Shrink Small-Outline (PW)	1A5 [] 11 14 [] 2 <u>A1</u>				
Packages	GND 12 13 20E				

description

The SN74CBTLV3384 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 5-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 5-bit bus switches or one 10-bit bus switch. When \overline{OE} is low, the associated 5-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3384 is characterized for operation from -40°C to 85°C.

(each 5-bit bus switch)								
INP	UTS	INPUTS/OUTPUTS						
1 <u>0E</u> 2 <u>0E</u>		1B1–1B5	2B1–2B5					
L	L	1A1–1A5	2A1–2A5					
L	н	1A1–1A5	Z					
Н	L	Z	2A1–2A5					
Н	н	Z	Z					

FUNCTION TABLE (each 5-bit bus switch)



SCDS059B - MARCH 1998 - REVISED SEPTEMBER 1998

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		. –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		–50 mA
Package thermal impedance, θ_{IA} (see Note 2):	DBQ package	103°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
VIH	High lovel control input veltage	V_{CC} = 2.3 V to 2.7 V	1.7		v
	High-level control linput voltage	V _{CC} = 2.7 V to 3.6 V	2		
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			0.7	V
VIL	Low-level control input voltage	$V_{CC} = 2.7 V \text{ to } 3.6 V$		0.8	v
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
VIK		$V_{CC} = 3 V,$	lı = –18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±1	μA
l _{off}		$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 3.6 \text{ V}$				10	μΑ
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆lCC [‡]	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0				4.5		pF
C _{io(OFF)}		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$			10		pF
		$V_{CC} = 2.3 V,$	$\mathcal{V}_{\mathcal{V}} = 0$	lı = 64 mA		5	8	
			V] = 0	lı = 24 mA		5	8	
r _{on} §			V _I = 1.7 V,	lı = 15 mA		27	40	0
			$\lambda = 0$	l _l = 64 mA		5	7	52
		$V_{CC} = 3 V$	V] = 0	l _l = 24 mA		5	7	
			V _I = 2.4 V,	lj = 15 mA		10	15	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡]This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER			V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		(0011 01)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.35		0.25	ns
t _{en}	OE	A or B	1	5	1	4.3	ns
tdis	ŌE	A or B	1	5.5	1	5.5	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2 ns, t_f ≤ 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



SCDS059B - MARCH 1998 - REVISED SEPTEMBER 1998



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tp_I H and tp_H are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms



SN74CBTLV3857 LOW-VOLTAGE 10-BIT FET BUS SWITCH WITH INTERNAL PULLDOWN RESISTORS SCD5085 – OCTOBER 1998

- DBQ, DGV, DW, OR PW PACKAGE Enable Signal Is SSTL_2 Compatible (TOP VIEW) Flow-Through Architecture Optimizes PCB Layout VREFL 24 Vcc Designed to Be Used With 200 Mbit/s A1 [23 OE 2 Double Data Rate (DDR) SDRAM A2 🛛 3 22 🛛 B1 Applications A3 4 B2 21 • Switch On-State Resistance Is Designed to B3 A41 20 5 Eliminate the Series Resistor to the DDR A5 6 19 Β4 **SDRAM** B5 A6 7 18 A7 🛛 8 П B6 17 Internal 10-kΩ Pulldown Resistors to A8 🛛 16 B7 9 Ground on the B Port 15 B8 A9 10 • Internal 50-kΩ Pullup Resistor on the A10 11 14 🛛 B9 **Output-Enable Input** GND 12 13 B10 • Package Options Include Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW),
- description

Packages

and Thin Shrink Small-Outline (PW)

This 10-bit FET bus switch is designed for 3-V to 3.6-V V_{CC} operation and SSTL_2 output-enable (\overline{OE}) input levels.

When \overline{OE} is low, the 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

The FET switch on-state resistance is designed to replace the series terminating resistor in the SSTL_2 data path.

The CBTLV3857 is characterized for operation from -40°C to 85°C.

INF O	PUT E	FUNCTION
L	-	A port = B port
ŀ	ł	Disconnect



SN74CBTLV3857 LOW-VOLTAGE 10-BIT FET BUS SWITCH WITH INTERNAL PULLDOWN RESISTORS SCDS085 - OCTOBER 1998

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range (OE only), V _I (see Note 1)		. –0.5 V to V _{CC} + 0.5 V
Input voltage range (except OE), VI (see Note	1)	–0.5 V to 4.6 V
Continuous channel current		48 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		
Package thermal impedance, θ_{JA} (see Note 2)	: DBQ package	103°C/W
	DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



SN74CBTLV3857 LOW-VOLTAGE 10-BIT FET BUS SWITCH WITH INTERNAL PULLDOWN RESISTORS

SCDS085 - OCTOBER 1998

recommended operating conditions (see Note 3)

		MIN	NOM	МАХ	UNIT
Vcc	Supply voltage	3	3.3	3.6	V
VREF	Reference voltage (0.38 \times V _{CC})	1.15	1.25	1.35	V
VIH	AC high-level control input voltage	V _{REF} + 350 mV			V
VIL	AC low-level control input voltage			V _{REF} – 350 mV	V
VIH	DC high-level control input voltage	V _{REF} + 180 mV			V
VIL	DC low-level control input voltage			V _{REF} – 180 mV	V
Т _А	Operating free-air temperature	-40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 3 V,	I _I = -18 mA				-1.2	V
	ŌĒ						±1	mA
	A port						±5	μA
''	B port	VCC = 3.0 V,	AL = ACC OL GIAD				±1	mA
	VREF						±5	μA
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$				mA
Ci	Control inputs	VI = 3 V or 0						pF
C _{io(OFF}	-)	V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
r _{on} ‡		V _{CC} = 3 V	$V_{\parallel} = 0,$	l _l = 24 mA				
			V _I = 0.9 V,	lj = 24 mA				Ω
			V _I = 1.25 V,	lj = 24 mA				
			V _I = 1.6 V,	lı = 24 mA				
roff		$V_{CC} = 0$	-					МО
		V _{CC} = 3 V to 3.6 V,	Vj = 1.65 V					17177

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25° C.

[‡] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V MIN MAX	UNIT
t _{pd} §	A or B	B or A		ns
t _{en}	ŌĒ	A or B		ns
^t dis	ŌĒ	A or B		ns

§ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).



SN74CBTLV3857 LOW-VOLTAGE 10-BIT FET BUS SWITCH WITH INTERNAL PULLDOWN RESISTORS

SCDS085 - OCTOBER 1998





- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 1.25 ns/V, $t_f \le 1.25 \text{ ns/V}.$
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tp71 and tp7H are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCDS041C - DECEMBER 1997 - REVISED OCTOBER 1998

- Functionally Equivalent to QS3861
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBTLV3861 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit bus switch. When output enable (\overline{OE}) is low, the 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

DGV, DW, OR PW PACKAGE (TOP VIEW)						
NC [A1 [A2 [A3 [A5 [A6 [A7 [A8 [A9 [A10]	(TOP 1 2 3 4 5 6 7 8 9 10 11	24 23 22 21 20 19 18 17 16 15 14	V _{CC} OE B1 B2 B3 B4 B5 B6 B7 B8 B9			
GND [12	13	B10			

NC - No internal connection

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3861 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE					
	FUNCTION				
L	A port = B port				
н	Disconnect				



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logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2)	: DGV package	139°C/W
	DW package	81°C/W
	PW package	120°C/W
Storage temperature range, T _{stg}		. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

2.3 3.6	V
.7	V
2] `
0.7	V
0.8	v
40 85	°C
_	2 0.7 0.8 -40 85

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
VIK		$V_{CC} = 3 V,$	lı = –18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_{I} = V_{CC} \text{ or } GND$				±1	μA
loff		$V_{CC} = 0,$	V_{I} or $V_{O}=0$ to 3.6 V				10	μΑ
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆lCC [‡]	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0						pF
Cio(OFF	=)	$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
			$V_{i} = 0$	lı = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	VI = 0	lı = 24 mA				
r _{on} §			V _I = 1.7 V,	lı = 15 mA				0
			$\lambda = 0$	l _l = 64 mA				52
		$V_{CC} = 3 V$	V] = 0	l _l = 24 mA				
			V _I = 2.4 V,	lj = 15 mA				

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡] This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO (OUTPUT)	V _{CC} = ± 0.2	2.5 V 2 V	V _{CC} = ± 0.3	3.3 V 3 V	UNIT
		(0011 01)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
ten	ŌĒ	A or B					ns
t _{dis}	ŌĒ	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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D - ----

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- **5**-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTLV16210 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 10-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV16210 is characterized for operation from -40° C to 85° C.

DGG, DGV, OR DL PACKAGE					
(TOP VIEW)					
NC [1 U	48] 1 <u>0E</u>		
1A1 [2	47] 2 <u>0E</u>		
1A2 [3	46] 1B1		
1A3 [4	45] 1B2		
1A4 [5	44] 1B3		
1A5 [6	43] 1B4		
1A6 [7	42] 1B5		
GND [8	41] GND		
1A7 [9	40] 1B6		
1A8 [10	39] 1B7		
1A9 [11	38] 1B8		
1A10 [12	37] 1B9		
2A1 [13	36]1B10		
2A2 [14	35] 2B1		
Vcc [15	34] 2B2		
2A3 [16	33] 2B3		
GND [17	32] GND		
2A4 [18	31] 2B4		
2A5 [19	30] 2B5		
2A6 [20	29] 2B6		
2A7 [21	28] 2B7		
2A8 [22	27] 2B8		
2A9 [23	26] 2B9		
2A10 [24	25]2B10		

NC – No internal connection

FUNCTION TABLE (each 10-bit bus switch)

	FUNCTION
L	A port = B port
Н	Disconnect

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logic diagram (positive logic)



PRODUCT PREVIEW similar

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Continuous channel current		122 m
		120 IIIA
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	89°C/W
	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, T _{stg}	·	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
	High lovel control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
	High-level control input voltage	V_{CC} = 2.7 V to 3.6 V	2		v
Ma	Low lovel control input veltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
VIL	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	v
ТĄ	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITI	ONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 3 V,	lj = -18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±1	μA
l _{off}		$V_{CC} = 0,$	V_{I} or V_{O} = 0 to 3.6 V	1			10	μΑ
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆lcc [‡]	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
			$\lambda = 0$	lj = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	VI = 0	lj = 24 mA				
. 8			V _I = 1.7 V,	l _l = 15 mA				0
^r on ³			$\lambda = 0$	lj = 64 mA				32
		$V_{CC} = 3 V$ $V = 0$	v] = 0	II = 24 mA				
			$V_{ } = 2.4 V,$	l _l = 15 mA				

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER			V _{CC} = 2 ± 0.2	2.5 V 2 V	V _{CC} = ± 0.3	3.3 V 3 V	UNIT
	(14601)		MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
t _{en}	ŌĒ	A or B					ns
^t dis	ŌĒ	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. tpLz and tpHz are the same as tdis.

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



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- **5**-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTLV16211 provides 24 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 12-bit bus switches or one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV16211 is characterized for operation from -40° C to 85° C.

DGG, DGV, OR DL PACKAGE				
	(TOP VI	EW)		
		56		
	2	55		
142	3	54	11B1	
143	4	53	11B2	
1 4 4	5	52	1 _{1B3}	
145	6	51	11B4	
146	3 7	50	1B5	
GND	8	49		
1A7 [9	48	1B6	
1A8 🛛	10	47	1B7	
1A9 🛛	11	46	1B8	
1A10 🛛	12	45	1B9	
1A11 🛛	13	44]1B10	
1A12	14	43]1B11	
2A1 🛛	15	42]1B12	
2A2 🛛	16	41	2B1	
v _{cc} [17	40	2B2	
2A3 🛛	18	39	2B3	
GND [19	38	GND	
2A4 🛛	20	37	2B4	
2A5 🛛	21	36	2B5	
2A6	22	35	2B6	
2A7 🛓	23	34	2B7	
2A8 L	24	33	2B8	
2A9 L	25	32	2B9	
2A10	26	31	2B10	
2A11	27	30	2B11	
2A12	28	29	2B12	

NC - No internal connection

FUNCTION TABLE				
(each 12-bit bus switch)				
	FUNCTION			

-

	FUNCTION
L	A port = B port
н	Disconnect



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logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		. –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT					
Vcc	Supply voltage	2.3	3.6	V					
	High-level control input voltage $\frac{V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}}{V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}}$			V					
VIH				v					
VIL	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V					
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			v					
TA	Operating free-air temperature	-40	85	°C					
NOTEO									

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
VIK		$V_{CC} = 3 V,$	lj = -18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±1	μΑ
l _{off}		$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 3.6 \text{ V}$				10	μΑ
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆lCC [‡]	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{io(OFF)}		$V_{O} = 3 V \text{ or } 0,$	$\overline{OE} = V_{CC}$					pF
		$V_{CC} = 2.3 V,$	V _I = 0	lı = 64 mA				
				lı = 24 mA				
r _{on} §			V _I = 1.7 V,	l _l = 15 mA				0
			N 0	lj = 64 mA				22
		$V_{CC} = 3 V$	v] = 0	lı = 24 mA				
			V _I = 2.4 V,	l _l = 15 mA				

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡]This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER			V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
t _{en}	ŌĒ	A or B					ns
tdis	ŌĒ	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms





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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



SCDS044D - DECEMBER 1997 - REVISED NOVEMBER 1998

 4-Ω Switch Connection Between Two Ports Isolation Under Power-Off Conditions 	DGG, DGV, OR DL PACKA (TOP VIEW)	GE
Break-Before-Make Feature		
Package Options Include Plastic Thin	1A1 2 55 S2	
Shrink Small-Outline (DGG), Thin Very	1A2 🛛 3 54 🖸 1B1	
Small-Outline (DGV), and 300-mil Shrink	2A1 4 53 1 1B2	
Small-Outline (DL) Packages	2A2 4 5 52 2B1	
dependention	3A1 4 6 51 2B2	
description	3A2 U 7 50 U 3B1	
The SN74CBTLV16212 provides 24 bits of	GND 49 GND)
high-speed bus switching or exchanging. The low	4A1 J 9 48 J 3B2	
on-state resistance of the switch allows	4A2 4 10 47 4B1	
connections to be made with minimal propagation	5A1 L 11 46 4B2	
delay.	5A2 45 5B1	
The device encycles on a 24 bit bus switch or a	6A1 Ц 13 44 U 5B2	
12 bit bue exchanger which provides date	6A2 41 43 6B1	
2-bit bus exchanger, which provides data	7A1 42 6B2	
data coloct (S0, S1, S2) terminals	7A2 41 7B1	
	V _{CC} 17 40 7B2	
The SN74CBTLV16212 is specified by the	8A1 U 18 39 U 8B1	
break-before-make design to have no through	GND [] 19 38 [] GND)
current when switching directions.	8A2 U 20 37 U 8B2	
The SN74CBTI \/16212 is characterized for	9A1 U 21 36 U 9B1	
operation from -40° C to 85° C	9A2 U 22 35 U 9B2	
	10A1 Ц 23 34 [] 10B1	l
	10A2 U 24 33 D 10B2	2
	11A1 🛛 25 🛛 32 🗍 11B1	

	FUNCTION TABLE									
INPUTS			INPUTS/0	OUTPUTS	FUNCTION					
S2	S 1	S0	A1	A2	FUNCTION					
L	L	L	Z	Z	Disconnect					
L	L	Н	B1	Z	A1 port = B1 port					
L	Н	L	B2	Z	A1 port = B2 port					
L	Н	Н	Z	B1	A2 port = B1 port					
Н	L	L	Z	B2	A2 port = B2 port					
Н	L	Н	Z	Z	Disconnect					
н	Н	L	B1	B2	A1 port = B1 port A2 port = B2 port					
н	Н	Н	B2	B1	A1 port = B2 port A2 port = B1 port					

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31 11B2

30 12B1

29 12B2

11A2 226 12A1 27

12A2 🛛 28

SCDS044D - DECEMBER 1997 - REVISED NOVEMBER 1998

logic diagram (positive logic)





SCDS044D - DECEMBER 1997 - REVISED NOVEMBER 1998

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		. −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
	V _{CC} = 2.3 V to 2.7 V		1.7		V
VIН	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		v	
VIL	Low-level control input voltage $\frac{V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}}{V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}}$			0.7	V
				0.8	
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCDS044D - DECEMBER 1997 - REVISED NOVEMBER 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 3 V,	l _l = –18 mA				-1.2	V
l	$V_{CC} = 3.6 \text{ V}, \qquad V_{I} = V_{CC} \text{ or GND}$				±1	μA		
$V_{CC} = 0,$ $V_{I} \text{ or } V_{O} = 0 \text{ to } 3.6 \text{ V}$				10	μA			
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆ICC [‡]	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	VI = 3 V or 0						pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$					pF
		$V_{CC} = 2.3 V,$	V ₁ = 0	lı = 64 mA				
				lı = 24 mA				
. 8			V _I = 1.7 V,	l _l = 15 mA				0
rons			$\lambda t = 0$	lj = 64 mA				52
		$V_{CC} = 3 V$	v] = 0	lj = 24 mA				
			$V_{I} = 2.4 V,$	lj = 15 mA				

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), $T_A = 25^{\circ}C$.

[‡] This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		(001701)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
^t pd	S	B or A					ns
t _{en}	S	A or B					ns
^t dis	S	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).


SN74CBTLV16212 LOW-VOLTAGE 24-BIT FET BUS-EXCHANGE SWITCH

SCDS044D - DECEMBER 1997 - REVISED NOVEMBER 1998



- - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tPZL and tPZH are the same as ten.
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBTLV16212 LOW-VOLTAGE 24-BIT FET BUS-EXCHANGE SWITCH

SCDS044D - DECEMBER 1997 - REVISED NOVEMBER 1998



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tPZL and tPZH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



SCDS060B - MARCH 1998 - REVISED OCTOBER 1998

	SCDS060B - MARCH 1998 -	- KE V
 4-Ω Switch Connection Between Two Ports Isolation Under Power-Off Conditions 	DGG PACKAGE (TOP VIEW)	
Break-Before-Make Feature		IR1
Backagod in Plastic Thin Shrink		IB2
Small-Outline Package		
Sman-Outline i ackage		-/\ 3B1
description	4B1 0 5 60 0 3	3B2
	4B2 1 6 59 1 4	1A
The SN74CBTLV16235 is an 18-bit 1-of-2 FET	5A 1 7 58 1 5	5B1
multiplexer/demultiplexer used in applications in	6B1 1 8 57 1 5	5B2
which two separate data paths must be	6B2 19 56 16	6A
multiplexed onto, or demultiplexed from, a single		7B1
path. This device can be used for memory	8B1 🛛 11 54 🗍 7	7B2
niterieaving, where two different barries of memory	8B2 🛛 12 53 🗍 8	3A
need to be addressed simulaneously.	GND 🛛 13 52 🗍 🤇	GND
The device is organized as a dual 9-bit 1-of-2	V _{CC} [] 14 51] \	/CC
multiplexer/demultiplexer with separate control	9A 🛛 15 50 🕽 9	9B1
inputs. It can be used as two 9-bit	10B1 🚺 16 49 🗍 9	9B2
multiplexer/demultiplexers or as one 18-bit	10B2 [17 48] 1	10A
multiplexer/demultiplexer. Two select (S0 and S1)	11A 🛛 18 47 🗋 1	I1B1
inputs control the data flow. When the test (10 and	12B1 [19 46] 1	11B2
11) Inputs are asserted, port A is connected to	12B2 [20 45] 1	12A
driven with a 5 V CMOS a 5 V TTL a low veltage	13A [] ₂₁ 44 [] 1	I3B1
TTL or an SSTL 2 driver	14B1 [22 43] 1	13B2
TTL, OF AN SSTL_S UNVEL	14B2 [23 42] 1	14A
The SN74CBTLV16235 is specified by the	15A 🛛 24 41 🗋 1	15B1
break-before-make design to have no through	16B1 2 5 40 1	15B2
current when switching directions.	16B2 [] ₂₆ 39 [] 1	16A
The SN74CBTLV16235 is characterized for	17A [] 27 38 [] 1	17B1
operation from -40°C to 85°C.		17B2
	10001	

PRODUCT PREVIEW

FUNCTION TABLE
(each 9-bit multiplexer/demultiplexer)

18B2 29

T0 🚺 31

T1 32

36 18A

35 GND

34 S0 33 S1

INP	UTS	FUNCTION			
Т	S	FUNCTION			
L	L	A port = B1 port			
L	Н	A port = B2 port			
н	Х	A port = B1 port = B2 port			



SCDS060B - MARCH 1998 - REVISED OCTOBER 1998

logic diagram (positive logic)



SCDS060B - MARCH 1998 - REVISED OCTOBER 1998

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	. –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	. –0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2)	73°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	V _{CC} Supply voltage				V
VIH	$V_{CC} = 2.3$ V		1.7		V
	High-level control liput voltage	2		v	
VIL	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$				v
Т _А	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS		ONS	MIN	TYP†	MAX	UNIT		
VIK		V _{CC} = 3 V,	I _I = -18 mA				-1.2	V
l		V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$				±5	μΑ
loff		V _{CC} = 0,	V_{I} or $V_{O} = 0$ to 3.6	V			10	μA
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC} \text{ or } GND$			10	μA
∆lcc [‡]	Control input	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control input	VI = 3 V or 0						pF
C _{io(OFF)}		V _O = 3 V or 0						pF
			$\lambda = 0$	lj = 64 mA				
r _{on} §		$V_{CC} = 2.3 V$, TYP at $V_{CC} = 2.5 V$	VI = 0	II = 24 mA				
		00	V _I = 1.7 V,	l _l = 15 mA				0
			$V_{i} = 0$	lı = 64 mA				52
		$V_{CC} = 3 V$	vI=0	lı = 24 mA				
			V _I = 2.4 V,	l _l = 15 mA				

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡]This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A					ns
t _{en}	S	A or B					ns
^t dis	S	A or B					ns
^t en	Т	A or B					ns
^t dis	Т	A or B					ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



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NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



SN74CBTLV16292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

- SCDS055C MARCH 1998 REVISED NOVEMBER 1998
- 4-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTLV16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1 and R_{INT} is connected to port B2. When S is high, port A is connected to port B2 and R_{INT} is connected to port B1.

The SN74CBTLV16292 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R _{INT} = B2 port
н	A port = B2 port R _{INT} = B1 port

DGG, DGV, OR DL PACKAGE						
	(TOP V	IEW)			
~ [٦				
	1	50				
	2	55				
	3	54				
	4	53				
	5	52				
	6	51				
	1	50				
	8	49				
4A L	9	48	U 3B2			
	10	47	U 4B1			
5A L	11	46	H 4B2			
	12	45				
6A L	13	44	15B2			
NC	14	43	L 6B1			
7A L	15	42	6B2			
NC	16	41	17B1			
Vcc	17	40	17B2			
8A L	18	39	8B1			
GND	19	38	GND			
ΝСЦ	20	37	8B2			
9A L	21	36	9B1			
NC	22	35	9B2			
10A 🛛	23	34	010B1			
NC	24	33	0 10B2			
11A 🛛	25	32	11B1			
NС [26	31	11B2			
12A 🛛	27	30	12B1			
ис [28	29	12B2			

NC - No internal connection



SN74CBTLV16292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS SCDS055C - MARCH 1998 - REVISED NOVEMBER 1998

logic diagram (positive logic)



PRODUCT PREVIEW

simplified schematic, each FET switch





SN74CBTLV16292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS055C - MARCH 1998 - REVISED NOVEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	V _{CC} Supply voltage			
	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	Notice the set of the			v
VIL	$V_{CC} = 2.3 \text{ V} \text{ to } 2.7 \text{ V}$		0.7	V
	Low-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			v
T _A Operating free-air temperature				°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITI	ONS	MIN TYP [‡] MAX		UNIT	
VIK		V _{CC} = 3 V,	l _l = –18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_{I} = V_{CC} \text{ or } GND$				±1	μA
l _{off}		$V_{CC} = 0,$	V_{I} or $V_{O} = 0$ to 3.6	6 V			10	μA
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆lCC§	Control input	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control input	V _I = 3 V or 0						pF
Cio(OFF))	$V_{O} = 3 V \text{ or } 0$						pF
R _{INT}	B1 or B2	V _{CC} = 3.3 V,	I _O = 4 mA			500		Ω
			$\lambda = 0$	lj = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$	VI = 0	lj = 24 mA				
. ¶			V _I = 1.7 V,	lj = 15 mA				0
'on"			V/- 0	l _l = 64 mA				52
		$V_{CC} = 3 V$	v] = 0	lj = 24 mA				
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBTLV16292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPLIT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN N	MAX	MIN	MAX	
t _{pd} †	A or B	B or A					ns
t _{en}	S	A or B					ns
^t dis	S	A or B					ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		то (OUTPUT) -	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(INFOT)		MIN MAX	MIN MAX	
t _{pd} †	A or B	B or A			ns
ten	S	A or B			ns
^t dis	S	A or B			ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics, $T_A = 0^{\circ}C$ to 70°C (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	DESCRIPTION	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MAX	MIN	MAX	
t _{mbb} ‡	Make-before-break time					ns

[‡]The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



SN74CBTLV16292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULL DOWN RESIST

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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tPZL and tPZH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBTLV16292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

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NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



SN74CBTLV162292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS056C – MARCH 1998 – REVISED NOVEMBER 1998

DGG, DGV, OR DL PACKAGE

(TOP VIEW)

S

1A L

2

56 🛛 NC

55 🛛 NC

- 4-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- A-Port Inputs/Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

NOTE: For order entry: The DGG package is abbreviated to G, and the DGV package is abbreviated to V.

description

The SN74CBTLV162292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1 and R_{INT} is connected to port B2. When S is high, port A is connected to port B2 and R_{INT} is connected to port B1.

The A-port inputs/outputs include equivalent $25 \cdot \Omega$ series resistors to reduce overshoot and undershoot.

The SN74CBTLV162292 is characterized for operation from -40° C to 85° C.

			h .
NC	3	54	1B1
2A	4	53	1B2
NC	5	52	2B1
3A [6	51	2B2
NC	7	50	3B1
GND	8	49	GND
4A	9	48	3B2
NC	10	47	4B1
5A	11	46	4B2
NC [12	45	5B1
6A [13	44	5B2
NC [14	43	6B1
7A [15	42	6B2
NC [16	41	7B1
v _{cc} [17	40	7B2
8A [18	39	8B1
GND	19	38	GND
NC	20	37	8B2
9A [21	36	9B1
NC [22	35	9B2
10A	23	34	10B1
NC	24	33	10B2
11A [25	32]11B1
NC [26	31	11B2
12A [27	30	12B1
NC	28	29	12B2
			•

NC - No internal connection

FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R _{INT} = B2 port
н	A port = B2 port R _{INT} = B1 port



SN74CBTLV162292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS SCDS056C - MARCH 1998 - REVISED NOVEMBER 1998

logic diagram (positive logic)



PRODUCT PREVIEW

simplified schematic, each FET switch





SN74CBTLV162292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS056C – MARCH 1998 – REVISED NOVEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

⁺ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC} Supply voltage			3.6	V
VIH	V _{CC} = 2.3 V to 2.7 V	1.7		V
	V _{CC} = 2.7 V to 3.6 V	2		v
V _{IL} L	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v
T _A Operating free-air temperature			85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS		MIN	түр‡	MAX	UNIT	
VIK		V _{CC} = 3 V,	l _l = –18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_{I} = V_{CC} \text{ or } GND$				±1	μA
l _{off}		$V_{CC} = 0,$	V_{I} or $V_{O} = 0$ to 3.6	6 V			10	μA
ICC		V _{CC} = 3.6 V,	IO = 0,	$V_I = V_{CC}$ or GND			10	μA
∆ICC§	Control input	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control input	V _I = 3 V or 0						pF
C _{io(OFF)})	$V_{O} = 3 V \text{ or } 0$						pF
R _{INT}	B1 or B2	V _{CC} = 3.3 V,	I _O = 4 mA			500		Ω
			$V_{CC} = 2.3 V,$ TYP at Vcc = 2.5 V	lj = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$		lı = 24 mA				
			V _I = 1.7 V,	lj = 15 mA				0
^r on ^{II}			l _l = 64 mA				52	
		$V_{CC} = 3 V$	v] = 0	lj = 24 mA				
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), $T_A = 25^{\circ}C$.

§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBTLV162292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TO (OUTPUT) -	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A					ns
t _{en}	S	A or B					ns
^t dis	S	A or B					ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		то (OUTPUT) -	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(INFOT)		MIN MAX	MIN MAX	
t _{pd} †	A or B	B or A			ns
ten	S	A or B			ns
^t dis	S	A or B			ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics, $T_A = 0^{\circ}C$ to 70°C (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	DESCRIPTION	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MAX	MIN	MAX	
t _{mbb} ‡	Make-before-break time					ns

[‡]The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



SN74CBTLV162292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESIST

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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tPZL and tPZH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74CBTLV162292 LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tPLH and tPHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



SN74CBTLV16800 LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS SCDS045E – DECEMBER 1997 – REVISED NOVEMBER 1998

DGG, DGV, OR DL PACKAGE

- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- B-Port Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBTLV16800 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as dual 10-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, a high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-k Ω resistor.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV16800 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 10-bit bus switch)			
	FUNCTION		
L	A port = B port		
н	A port = Z B port = BIASV		

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SN74CBTLV16800 LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS SCDS045E – DECEMBER 1997 – REVISED NOVEMBER 1998

logic diagram (positive logic)



simplified schematic, each FET switch





SN74CBTLV16800 LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPU SCDS045E - DECEMBER 1997 - REVISED NOVEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, v _{CC}		-0.5 V to 4.6 V
Bias voltage range, BIASV		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	89°C/W
	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC} Supply voltage			3.6	V
BIASV	Bias voltage	0	VCC	V
	High level central input voltage $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		v
VIH	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
	V _{CC} = 2.3 V to 2.7 V		0.7	V
۷IL	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 3 V,	l _l = –18 mA				-1.2	V
Ц		V _{CC} = 3.6 V,	$V_{I} = V_{CC} \text{ or } GND$				±1	μA
loff		V _{CC} = 0,	V_{I} or V_{O} = 0 to 3.6 V				10	μA
IO		V _{CC} = 3 V,	BIASV = 2.4 V,	V _O = 0	0.25			mA
ICC		V _{CC} = 3.6 V,	I _O = 0,	$V_I = V_{CC}$ or GND			10	μA
∆ICC§	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
Ci	Control inputs	V _I = 3 V or 0						pF
C _{O(OFF)}		V _O = 3 V or 0,	Switch off					pF
			$V_{I} = 0$	l _l = 64 mA				
		$V_{CC} = 2.3 V,$ TYP at $V_{CC} = 2.5 V$		I _I = 24 mA				
			V _I = 1.7 V,	lj = 15 mA				0
"on "		V _{CC} = 3 V	V _I = 0	lj = 64 mA				
				I _I = 24 mA				
			V _I = 2.4 V,	lj = 15 mA				

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBTLV16800 LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS SCDS045E - DECEMBER 1997 - REVISED NOVEMBER 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	TEST FROM CONDITIONS (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT		
			(001101)	MIN MAX	MIN MAX		
t _{pd} †		A or B	B or A			ns	
^t PZH	BIASV = GND	ŌĒ					20
^t PZL	BIASV = 3 V		AOIB			115	
^t PHZ	BIASV = GND	ŌE	A or P				
^t PLZ	BIASV = 3 V		AUD			115	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CI includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{Dd} .

Figure 1. Load Circuit and Voltage Waveforms



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns. D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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Texas Instruments Crossbar Switches

SCDA001A July 1995



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What Are Texas Instruments Crossbar Switches?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an n-channel MOS transistor driven by a CMOS gate. When enabled, the n-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on-state resistance of approximately 5 Ω and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at ≈ 1 V less than the gate potential, regardless of the level at the input pin. This is one of the n-channel transistor characteristics (see Figures 1 and 2). Note the ≈ 1 -V difference between the gate (V_{CC}) and the source (V_O) at any point on the graph.



Figure 1. Output Voltage Versus Supply Voltage





The on-state resistance (r_{on}) increases gradually with V_I until V_I approaches $V_{CC} - 1$ V, where r_{on} rapidly increases, clamping V_O at $V_{CC} - 1$ V (see Figure 3). Also, by the nature of the n-channel transistor design, the input and output terminals are fully isolated when the transistor is off. Leakage and capacitance are to ground and not between input and output, which minimizes feedthrough when the transistor is off.



Figure 3. On-State Resistance Versus Input Voltage

Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided

These devices also can provide bidirectional 5-V to 3-V translation with minimal propagation delay or direction control, using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes gate voltage of 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source drop of 1 V, brings V_{O} to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

These devices consume very little current ($I_{CC} = 3 \mu A$). This current is not satisfactory for the diode to operate. Using a resistor from the cathode of the diode to GND allows more current from the supply voltage, causing the diode to operate and to clamp at the specified 4.3 V (see Figure 4). The recommended value of the resistor is 1 k Ω or less.



Figure 4. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems in which signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices also can replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on-state resistance and without relay-reliability problems.

Bus Switches Convert TTL Logic to Hot Card-Insertion Capability

This application is used mostly in systems that require hot card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and cannot be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., which do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first, followed by the signal pins, then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance cannot be achieved using CMOS logic since it contains p-channel transistors that provide an inherent diode between the I/O pins and V_{CC} . The diode is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground, leaving the bus disturbed.



Figure 5. ACL Direction of Current Flow When $V_{CC} = 0 V$

Another issue to consider is that, when V_{CC} is ramping, but still below the device-operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error does not occur.

There are two solutions to this problem; one is to use Texas Instruments BiCMOS technology (BCT) or advanced BiCMOS technology (ABT) families, since both ensure the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down.



Figure 6. No ABT Current Flow When $V_{CC} = 0 V$

The second solution is to use the Texas Instruments CBT family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed. The switch uses an n channel that prevents the current from flowing into the switch when powered down (see Figure 7). One device in particular, the SN74CBT6800, is designed specifically for hot card insertion. It has a built-in channel pullup tied to a bias voltage (BIASV) that is provided to ensure power up with the buses not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).



Figure 7. Hot Card-Insertion Application



 † I_{OL} > I_R, so the control signal can override the pullup resistor.

Figure 8. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple n-channel transistors, they are capable of providing several important bus functions, such as hot card insertion, near-zero-delay communication, 5-V to 3-V translation, and memory management in multiprocessor environments.

Acknowledgment

The author of this document is Ramzi Ammar.

SN74CBTS3384 Bus Switches Provide Fast Connection and Ensure Isolation

SCDA002A August 1996


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Introduction

Buses are the pathways for communication between the CPU, memory, and I/O ports in electronic systems. Today's standards demand both fast connection as well as isolation of these buses. Bus switches are usually used to address these demands because the use of a single MOSFET provides negligible propagation delay, low power dissipation and bidirectional switching; however, the use of a single transistor also can allow large negative undershoots below –1 V to cause unwanted switching and possible disruption of the bus. To prevent this problem from occurring, the SN74CBTS3384 bus switches are developed with Schottky diodes at the inputs that clamp any undershoot to approximately –300 mV (see Figure 1).



Figure 1. The SN74CBTS3384 With Schottky Diodes Attached at Both Ports

The Mechanics of the MOSFET Switch Leading to False Switching

The MOSFET is used for bus switches because of its enabling and disabling speed, its low on-state resistance, and its high off-state resistance. The substrate of the N-channel MOSFET is grounded and the two n-type doped regions are interchangeable. As shown in Figure 2, when a logic high is applied to the gate, the region with a voltage of 1V or more below the gate becomes the source and the other region the drain. At this point, the switch turns fully on and a signal flows from the input side. While this physical structure of the MOSFET provides bidirectional capability in a switch, it also allows large negative undershoots on either port to turn on a disabled switch.



The interchangeability of the source and drain provides bidirectional signal flow.

Figure 2. Switching Mechanics of the NMOS Switch

As Figure 3 shows, even though the switch is initially disabled and there is a logic low at the gate, large negative undershoots at the input cause the existing clamping diode to clamp to approximately -650 mV. Since this voltage is parallel to the gate-to-source voltage of the transistor and lasts for a few nanoseconds, the transistor starts conducting a certain amount of current. This causes a logic low to appear on the bus and disrupts any signals on it.



Output enable (OE) is high, but large negative undershoot causes NMOS switch to turn on.

Figure 3. Mechanics Behind False Switching

Disruption of the Bus

False switching can disrupt the bus in many ways. Bus switches connect two buses or several components on a bus when on, and isolates them when off. Because each component has a certain amount of capacitance, an unexpected connection loads the bus with additional capacitance. Under normal circumstances, a signal is given enough drive to charge the expected capacitance on the bus and then switch voltage levels at the receiver. A signal propagating on the disrupted line may not have enough drive to overcome the additional load capacitance. In fact, the logic low introduced to the bus by the false connection can absorb some of the drive current from the signal. In any case, the end result is signal weakening, loss of speed, and failure to switch voltage levels at the receiver. Figure 4A shows a transaction between a CPU and a RAM chip connected by switches A and B. When switch C is off, the data flow is uninterrupted. As shown in Figure 4B, switch C can turn on unexpectedly and connect the I/O port to the bus. This results in signal degradation and data loss.





Resulting bus interruption and data loss



False switching also can cause bus contention, a case occurring when two or more transmitters on a bus are active at the same time. If the logic levels of these outputs are different, a high current flows on the line, possibly damaging the line or the components connected to it. These problems can cause serious setbacks to the high performance and reliability demands of today's systems. The use of the SN74CBTS3384 bus switch helps prevent false switching and addresses many of these problems.

The SN74CBTS3384 Solution

The SN74CBTS3384 utilizes Schottky diode at the inputs to clamp undershoot to about 300 mV below ground (see Figure 5). With the gate grounded in the disabled state, the Schottky diode prevents the gate-to-source voltage from exceeding the threshold voltage of the NMOS transistor, thus preventing weak enabling. In addition, a disabled SN74CBTS3384 switch offers a very low capacitance of about 6 pF and very low leakage current. Figure 5 shows total leakage current of only 2 μ A. As a result, the disabled SN74CBTS3384 bus switch succeeds in isolating its output from any unwanted undershoots at the input. The buses are left uninterrupted and the signals on the buses are not disturbed.







Figure 6 shows the output of a disabled SN74CBT3384A (without Schottky diodes) as it turns on and follows the input to a negative level. This level is low enough to possibly disrupt the bus. Figure 6 also shows the SN74CBTS3384 where the Schottky diode prevents any switching throughout the wide input sweep and keeps the output at a steady level. Figure 7 shows the input current of the SN74CBTS3384 as the Schottky diode turns on, conducting about 10 mA from ground.



Figure 6. V_O vs V_I of the SN74CBTS3384 and a SN74CBT3384A in the Disabled State



Figure 7. Input Current vs V_I of SN74CBTS3384 in the Disabled State

Conclusion

The SN74CBTS3384 bus switch provides a high-speed, low-power solution to bus connection, while providing a reliable solution to bus isolation. As a result, buses function properly without any problematic interruptions and the high-performance demands of today's systems are easily reached.

Acknowledgment

The author of this report is Nalin Yogasundram.

5-V to 3.3-V Translation With the SN74CBTD3384

SCDA003B March 1997



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Introduction

The emergence of low-voltage technology has required existing 5-V systems to interact with 3.3-V systems. Issues concerning compatibility of the two systems in mixed-mode operation have created the need for 5-V to 3.3-V translation. Buffers and transceivers serve as effective translators. While providing additional drive, these devices also add propagation delay and require directional control. In cases where additional drive is not required, the solution that provides 5-V to 3.3-V translation, in addition to negligible propagation delay, lower power dissipation, and bidirectional bus switching, is the SN74CBTD3384 uses the inherent voltage drop of its MOSFET switch, coupled with an internal diode from V_{CC} to provide the necessary 5-V to 3.3-V translation (see Figure 1).



Figure 1. The SN74CBTD3384 Bus Switch Provides 5-V to 3.3-V Translation and Bidirectional Switching

The Need for 5-V to 3.3-V Translation

To realize the need for 5-V to 3.3-V translation, the I/O specifications for mixed-mode operation must be understood. Devices operating in this mode must have TTL-compatible output levels and be able to accept up to 5.5 V at the input. Figure 2 shows various interface levels for 5-V and 3.3-V families. While many 5-V and 3.3-V logic families have been designed with TTL-compatible interface levels and 5-V input tolerance, some CMOS families lack these features. Some 5-V CMOS outputs drive to 5 V; however, certain 3.3-V CMOS inputs do not tolerate 5 V. It is the incompatibility of the described input and output structures that creates the need for 5-V to 3.3-V translation.



[†] In accordance with JEDEC Standard 8-A for LV interface levels

Figure 2. Comparison of 5-V and 3.3-V Interface levels

The Mechanics of 5-V to 3.3-V Translation

The CBT bus switches consist of an N-channel MOSFET with its drain and source connected from input to output. The nominal value of the threshold of the MOSFET is 1 V. The MOSFET (Pass transistor) is on when the gate-to-source voltage (V_g) exceeds 1 V. A V_{CC} of 5 V connected to the gate, and a gate-to-source voltage drop of 1 V results in a maximum source voltage of about 4 V. This source voltage limitation, coupled with the transistor's typical on-state resistance of 5 Ω , gives the switch both 5-V to 4-V translation and low propagation delay. If the gate voltage is reduced lower than V_{CC} , the source will be limited to a voltage lower than 4 V. As shown in Figure 3, the SN74CBTD3384 has a diode from V_{CC} to the rest of the circuit. This diode voltage drop is 0.7 V from V_{CC} , which leads to 4.3 V at the gate of the Pass transistor. With the additional 1-V drop from gate to source, the typical output of the SN74CBTD3384 is 3.3 V. Additional diodes can be added to limit the output to even lower voltages. It is important to note that in some cases, the quiescent current (I_{CC}) flowing through the diode may not be enough to turn on the diode. A resistor (R) is added to ground to ensure enough bias current through the diode. The bidirectional nature of the switch is not sacrificed in this translation. A logic high from a 3.3-V device is relayed to the output untranslated. A 5-V receiver with TTL-compatible interface levels reads this signal as a valid high.



Figure 3. NMOS Switch of SN74CBTD3384 With Maximum VO of 3.5 V

SN74CBTD3384 Improves Upon Existing Methods for 5-V to 3.3-V Translation

An existing practice for 5-V to 3.3-V translation using a bus switch involves the diode external to the chip. For most purposes, this method provides a quick, effective solution for voltage reduction. But, with increased use of low-voltage technology, the use of smaller, more reliable parts becomes an important issue. The SN74CBTD3384 addresses this issue by integrating the diode and resistor internally into the chip. As a result, board space is reduced and the cost of external components is eliminated. The integration of the components into one chip also eliminates extra solder connections and makes testing easier. Noise sensitivity is decreased, as well as the chance of false switching. The modified control input threshold of the SN74CBTD3384 compensates for the diode drop from V_{CC} and retains the normal 5-V TTL input threshold. This further reduces the noise problem. As demonstrated by the preceding factors, the SN74CBTD3384 offers increased reliability.

Figure 4 shows a comparison between the SN74CBT3384A, SN74CBT3384A with a 1N916 external diode for voltage translation, and the SN74CBTD3384. The SN74CBTD3384 output follows the input closely, but reaches a maximum of approximately 3.45 V at a V_{CC} of 5.5 V. Even at an extreme input level of 7 V, the SN74CBTD3384 limits the output to 3.5 V. Figure 5 emphasizes the role of V_{CC} in limiting the output. As V_{CC} changes from 4.5 V to 5.5 V, so does the limit of the output.



Figure 4. V_O Versus V_I of SN74CBT3384A, SN74CBT3384A With 1N916 External Diode, and SN74CBTD3384



Figure 5. V_O Versus V_{CC} of the SN74CBTD3384

Conclusion

Lack of compatibility between certain 5-V and 3.3-V devices has driven the need for 5-V to 3.3-V translation. The standard method of using a bus switch to address this need has, historically, required an external diode. The SN74CBTD3384 bus switch is an improvement to this method because it provides reliable 5-V to 3.3-V translation and maintains its bidirectional capability, negligible propagation delay, and low power dissipation.

Acknowledgment

The author of this report is Nalin Yogasundram.

Implications of Slow or Floating CMOS Inputs

SCBA004C February 1998



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Introduction

In recent years, CMOS (AC/ACT, AHC/AHCT, ALVC, CBT, CBTLV, HC/HCT, LVC, LV/LV-A) and BiCMOS (ABT, ALVT, BCT, FB, GTL, and LVT) logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. The reason is obvious: power consumption is becoming a major issue in today's market. However, when designing systems using CMOS and BiCMOS devices, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer requires, as well as to design within the data-sheet specifications. Because data sheets do not cover the input behavior of a device in detail, this application report explains the input characteristics of CMOS and BiCMOS families in general. It also explains ways to deal with issues when designing with families in which floating inputs are a concern. Understanding the behavior of these inputs results in more robust designs and better reliability.

Characteristics of Slow or Floating CMOS Inputs

Both CMOS and BiCMOS families have a CMOS input structure. This structure is an inverter consisting of a p-channel to V_{CC} and an n-channel to GND as shown in Figure 1. With low-level input, the p-channel transistor is on and the n-channel is off, causing current to flow from V_{CC} and pulling the node to a high state. With high-level input, the n-channel transistor is on, the p-channel is off, and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region, causing the n-channel and the p-channel to turn on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 to 2 V). The supply current (I_{CC}) can rise to several milliamperes per input, peaking at approximately 1.5-V V_{I} (see Figure 2). This is not a problem when switching states within the data-sheet-specified input transition time limit specified in the recommended operating conditions table for the specific devices. Examples are shown in Figure 3.



Figure 1. Input Structures of ABT and LVT/LVC Devices



Figure 2. Supply Current Versus Input Voltage (One Input)

recommended operating conditions[†]

				MIN	MAX	UNIT
		ABT octals	ABT octals		5	
		ABT Widebus [™] and Widebus	;+ TM		10	
		AHC, AHCT			20	
		FB			10	
$\Delta t / \Delta v$	Input transition rise or fall rate	LVT, LVC, ALVC, ALVT			10	ns/V
		LV			100	
		LV-A	V _{CC} = 2.3 V to 2.7 V		200	
			V _{CC} = 3 V to 3.6 V		100	
			V_{CC} = 4.5 V to 5.5 V	20		
			V _{CC} = 2 V		1000	
tt	Input transition (rise and fall) time	HC, HCT	V _{CC} = 4.5 V		500	ns
		V _{CC} = 6 V			400	

 $^{\dagger}\,\text{Refer}$ to the latest TI data sheets for device specifications.

Figure 3. Input Transition Rise or Fall Rate as Specified in Data Sheets

Slow Input Edge Rate

With increased speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations. Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.

These functional problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 4). Because the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, inductive voltage spikes, V_{GND} , affect the way signals appear to the internal gate structures. For example, as the voltage at the device's ground node rises, the input signal, V_{I} ', appears to decrease in magnitude. This undesirable phenomenon can then erroneously change the output if a threshold violation occurs.

In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_{I} , at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge is repeatedly driven back through the threshold, causing the output to oscillate. Therefore, the maximum input transition time of the device should not be violated, so no damage to the circuit or the package occurs.



Figure 4. Input/Output Model

Floating Inputs

If a voltage between 0.8 V and 2 V is applied to the input for a prolonged period of time, this situation becomes critical and should not be ignored, especially with higher bit count and more dense packages (SSOP, TSSOP). For example, if an 18-bit transceiver has 36 I/O pins floating at the threshold, the current from V_{CC} can be as high as 150 mA to 200 mA. This is approximately 1 W of power consumed by the device, which leads to a serious overheating problem. This continuous overheating of the device affects its reliability. Also, because the inputs are in the threshold region, the outputs tend to oscillate, resulting in damage to the internal circuit over a long period of time. The data sheet shows the increase in supply current (ΔI_{CC}) when the input is at a TTL level [for ABT $V_I = 3.4$ V, $\Delta I_{CC} = 1.5$ mA (see Figure 5)]. This becomes more critical when the input is in the threshold region as shown in Figure 6.

These characteristics are typical for all CMOS input circuits, including microprocessors and memories.

For CBT or CBTLV devices, this applies to the control inputs. For FB and GTL devices, this applies to the control inputs and the TTL ports only.

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
∆lCC [‡]	ABT, AHCT	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at $V_{\mbox{CC}}$ or GND		1.5	
	CBT Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		2.5	mA
ΔI_{CC}^{\ddagger}	CBTLV Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND		750	μA
∆lCC‡	LVT			Other inputs at Version CND		0.2	m۸
	LVC, ALVC, LV	$v_{\rm CC} = 3 \ v_{10} \ 3.0 \ v_{\rm c}$				0.5	ША

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)[†]

[†]Refer to the latest TI data sheets for device specifications.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Figure 5. Examples of Supply-Current Change of the Input at TTL Level as Specified in Data Sheets



Figure 6. Supply Current Versus Input Voltage (36 Inputs)

As long as the driver is active in a transmission path or bus, the receiver's input is always in a valid state. No input specification is violated as long as the rise and fall times are within the data-sheet limits. However, when the driver is in a high-impedance state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus. Figure 7 is an example of a typical bus system. When all transceivers are inactive, the bus-line levels are undefined. When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*. The result is a considerable increase in power consumption and a risk of damaging all components on the bus. Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.



Figure 7. Typical Bidirectional Bus

Recommendations for Designing More-Reliable Systems

Bus Control

The simplest way to avoid floating inputs in a bus system is to ensure that the bus always is either active or inactive for a limited time when the voltage buildup does not exceed the maximum V_{IL} specification (0.8 V for TTL-compatible input). At this voltage, the corresponding I_{CC} value is too low and the device operates without any problem or concern (see Figures 2 and 4).

To avoid damaging components, the designer must know the maximum time the bus can float. First, assuming that the maximum leakage current is $I_{OZ} = 50 \,\mu\text{A}$ and the total capacitance (I/O and line capacitance) is $C = 20 \,\text{pF}$, the change in voltage with respect to time on an inactive line that exceeds the 0.8-V level can be calculated as shown in equation 1.

$$\Delta V / \Delta t = \frac{I_{OZ}}{C} = \frac{50 \ \mu A}{20 \ pF} = 2.5 \ V / \mu s$$
 (1)

The permissible floating time for the bus in this example should be reduced to 320 ns maximum, which ensures that the bus does not exceed the 0.8-V level specified. The time constant does not change when multiple components are involved because their leakage currents and capacitances are summed.

The advantage of this method is that it requires no additional cost for adding special components. Unfortunately, this method does not always apply because buses are not always active.

Pullup or Pulldown Resistors

When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components from being damaged or overheated. A pullup or a pulldown resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and, if its resistance is not chosen properly, a problem may occur. Usually, a 1-k Ω to 10-k Ω resistor is recommended. The maximum input transition time must not be violated when selecting pullup or pulldown resistors (see Figure 3). Otherwise, components may oscillate, or device reliability may be affected.



Figure 8. Inactive-Bus Model With a Defined Level

Assume that an active-low bus goes to the high-impedance state as modeled in Figure 8. C_T represents the device plus the bus-line capacitance and R is a pullup resistor to V_{CC} . The value of the required resistor can be calculated as shown in equation 2.

$$V(t) = V_{CC} - [e^{-t/RC_{T}} (V_{CC} - V_{i})]$$
(2)

Where:

R = pullup resistor

t = maximum input rise time as specified in the data sheets (see Figure 3).

Solving for R, the equation becomes:

$$R = \frac{t}{0.4 \times C_{\rm T}} \tag{3}$$

For multiple transceivers on a bus:

$$R = \frac{t}{0.4 \times C \times N}$$
(4)

Where:

C = individual component and trace capacitance

N = number of components connected to the bus

Assuming that there are two components connected to the bus, each with a capacitance C = 15 pF, requiring a maximum rise time of 10 ns/V and t = 15-ns total rise time for the input (2 V), the maximum resistor size can be calculated:

$$R = \frac{15 \text{ ns}}{0.4 \times 15 \text{ pF} \times 2} = 1.25 \text{ k}\Omega$$
(5)

This pullup resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is critical. Instead, use the bus-hold feature that is discussed in the next section. The overall advantage of using pullup resistors is that they ensure defined levels when the bus is floating and help eliminate some of the line reflections, because resistors also can act as bus terminations.

Bus-Hold Circuits

The most effective method to provide defined levels for a floating bus is to use Texas Instruments (TI[™]) built-in bus-hold feature on selected families or as an external component like the SN74ACT1071 and SN74ACT1073 (refer to Table 1).

DEVICE TYPE	BUS HOLD INCORPORATED
SN74ACT1071	10-bit bus hold with clamping diodes
SN74ACT1073	16-bit bus hold with clamping diodes
ABT Widebus+ (32 and 36 bit)	All devices
ABT Octals and Widebus	Selected devices only
AHC/AHCT Widebus	TBA (Selected devices only)
Low Voltage (LVT and ALVC)	All devices
LVC Widebus	All devices

Table 1. Devices With Bus Hold

Bus-hold circuits are used in selected TI families to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors. Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 9). To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor. The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.



Figure 9. Typical Bus-Hold Circuit

As mentioned previously in this section, TI offers the bus-hold capability as stand-alone 10-bit and 16-bit devices (SN74ACT1071 and SN74ACT1073) with clamping diodes to V_{CC} and GND for added protection against line reflections caused by impedance mismatch on the bus. Because purely ohmic resistors cannot be implemented easily in CMOS circuits, a configuration known as a transmission gate is used as the feedback element (see Figure 10). An n-channel and a p-channel are arranged in parallel between the input and the output of the buffer stage. The gate of the n-channel transistor is connected to V_{CC} and the gate of the p-channel is connected to GND. When the output of the buffer is high, the p-channel is on, and when the output is low, the n-channel is on. Both channels have a relatively small surface area — the on-state resistance from drain to source, R_{dson} , is about 5 k Ω .



Figure 10. Stand-Alone Bus-Hold Circuit (SN74ACT107x)

Assume that in a practical application the leakage current of a driver on a bus is $I_{OZ} = 10 \,\mu\text{A}$ and the voltage drop across the 5-k Ω resistance is $V_D = 0.8 \,\text{V}$ (this value is assumed to ensure a defined logic level). Then, the maximum number of components that a bus-hold circuit can handle is calculated as follows:

$$N = \frac{V_D}{I_{OZ} \times R} = \frac{0.8 V}{10 \ \mu A \times 5 \ k\Omega} = 16 \text{ components}$$
(6)

The 74ACT1071 and 74ACT1073 also provide clamping diodes as an added feature to the bus-hold circuit. These diodes are useful for clamping any overshoot or undershoot generated by line reflections. Figure 11 shows the characteristics of the diodes when the input voltage is above V_{CC} or below GND. At $V_I = -1V$, the diode can source about 50 mA, which can help eliminate undershoots. This can be very useful when noisy buses are a concern.



Figure 11. Diode Characteristics (SN74ACT107x)

TI also offers the bus-hold circuit as a feature added to some of the advanced-family drivers and receivers. This circuit is similar to the stand-alone circuit, with a diode added to the drain of the second inverter (ABT and LVT only, see Figure 12). The diode blocks the overshoot current when the input voltage is higher than V_{CC} ($V_I > V_{CC}$), so only the leakage current is present. This circuit uses the device's input stage as its first inverter; a second inverter creates the feedback feature. The calculation of the maximum number of components that the bus-hold circuit can handle is similar to the previous example. However, the advantage of this circuit over the stand-alone bus-hold circuit is that it eliminates the need for external components or resistors that occupy more area on the board. This becomes critical for some designs, especially when wide buses are used. Also, because cost and board-dimension restrictions are a major concern, designers prefer the easy fix: drop-in replaceable parts. TI offers this feature in most of the commonly used functions in several families (refer to Table 1 for more details).



Figure 12. Input Structure of ABT/LVT and ALVC/LVC Families With Bus-Hold Circuit

Figure 13 shows the input characteristics of the bus-hold circuit at 3.3-V and 5-V operations, as the input voltage is swept from 0 to 5 V. These characteristics are similar in behavior to a weak driver. This driver sinks current into the part when the input is low and sources current out of the part when the input is high. When the voltage is near the threshold, the circuit tries to switch to the other state, always keeping the input at a valid level. This is the result of the internal feedback circuit. The plot also shows that the current is at its maximum when the input is near the threshold. I_{I(hold)} maximum is approximately 25 μ A for 3.3-V input and 400 μ A for 5-V input.





When multiple devices with bus-hold circuits are driven by a single driver, there may be some concern about the ac switching capability of the driver becoming weaker. As small drivers, bus-hold circuits require an ac current to switch them. This current is not significant when using TI CMOS and BiCMOS families. Figure 14 shows a 4-mA buffer driving six LVTH16244 devices. The trace is a 75- Ω transmission line. The receivers are separated by 1cm, with the driver located in the center of the trace. Figure 15 shows the bus-hold loading effect on the driver when connected to six receivers switching low or high. It also shows the same system with the bus-hold circuit disconnected from the receivers. Both plots show the effect of bus hold on the driver's rise and fall times. Initially, the bus-hold circuit tries to counteract the driver, causing the rise or fall time to increase. Then, the bus-hold circuit changes states (note the crossover point), which helps the driver switch faster, decreasing the rise or fall time.



Figure 14. Driver and Receiver System



Figure 15. Output Waveforms of Driver With and Without Receiver Bus-Hold Circuit

Figure 16 shows the supply current (I_{CC}) of the bus-hold circuit as the input is swept from 0 to 5 V. The spike at about 1.5-V V_I is due to both the n-channel and the p-channel conducting simultaneously. This is one of the CMOS transistor characteristics.



Figure 16. Bus-Hold Circuit Supply Current Versus Input Voltage

The power consumption of the bus-hold circuit is minimal when switching the input at higher frequencies. Figure 17 shows the power consumed by the input at different frequencies, with or without bus hold. The increase in power consumption of the bus-hold circuit at higher frequencies is not significant enough to be considered in power calculations.



Power Plot of the Input With Bus Hold

Figure 17. Input Power With and Without Bus Hold at Different Frequencies

Figure 18 shows the data-sheet dc specifications for bus hold. The first test condition is the minimum current required to hold the bus at 0.8 V or 2 V. These voltages meet the specified low and high levels for TTL inputs. The second test condition is the maximum current that the bus-hold circuit sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input voltage approaches the rail voltage. The output leakage currents, I_{OZH} and I_{OZL} , are insignificant for transceivers with bus hold because a true leakage test cannot be performed due to the existence of the bus-hold circuit. Because the bus-hold circuit behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with the bus-hold feature only and does not apply to buffers. All LVT, ABT Widebus+, and selected ABT octal and Widebus devices have the bus-hold feature (refer to Table 1 or contact the local TI sales office for more information).

electrical characteristics over recommended operating free-air temperature range (for families with bus-hold feature) $\!\!\!\!^\dagger$

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT		
					V _I = 0.8 V	75		
			vCC = 3 v	V _I = 2 V	-75			
l _{l(hold)}	Data inputs or I/Os	LVC, ALVC	V _{CC} = 3.6 V,	VI = 0 to 3.6 V		±500	μΑ	
l ` ´	01 1/03	ABT Widebus+ and	ABT $V_{CC} = 4.5 V$	V _I = 0.8 V	100			
		selected ABT		V _I = 2 V	-100			
^I OZH ^{/I} OZL	Transceivers with bus hold	ABT	This test is not a true I _{OZ} test because bus hold always is active on an I/O pin. Bus hold tends to supply a current that is opposite in direction to the output leakage current.	This test is not a true I _{OZ} test because bus hold always is active on an I/O pin. Bus hold		+1		
		LVT, LVC, ALVC		tends to supply a current the direction to the output leak	t that is opposite in akage current.		±1	μΑ
	Buffers	ABT	This test is a true I _{OZ} tes not exist on an output pin	st since bus hold does		±10		
	with bus hold	LVT, LVC, ALVC		not exist on an output pin.	า.		±5	

[†]Refer to the latest TI data sheets for device specifications.

Figure 18. Example of Data-Sheet Minimum Specification for Bus Hold

Summary

Floating inputs and slow rise and fall times are important issues to consider when designing with CMOS and advanced BiCMOS families. It is important to understand the complications associated with floating inputs. Terminating the bus properly plays a major role in achieving reliable systems. The three methods recommended in this application report should be considered. If it is not possible to control the bus directly, and adding pullup or pulldown resistors is impractical due to power-consumption and board-space limitations, bus hold is the best choice. TI designed bus hold to reduce the need for resistors used in bus designs, thus reducing the number of components on the board and improving the overall reliability of the system.

3.3-V to 2.5-V Translation With Texas Instruments Crossbar Technology

SCDA004A April 1998



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Introduction

The Texas Instruments (TI[™]) crossbar-technology (CBT) family is known for its multipurpose use in the design arena. It is used in almost every personal computer, server, workstation, and telecom application in the industry. CBT is an easy and low-cost solution for systems that require:

- Bus isolation
- Bus swapping in a multiprocessor/memory environment
- Live insertion
- 5-V to 3.3-V translation
- 3.3-V to 2.5-V translation

Translation from 3.3 V to 2.5 V is accomplished easily; however, reliable translation from 2.5 V to 3.3 V cannot be achieved with the existing CBT family because there is no noise margin for the high-state switching.

2.5-V and 3.3-V Switching Standards

Figure 1 shows the 3.3-V and 2.5-V switching thresholds.



Figure 1. 3.3-V and 2.5-V V_{CC} Thresholds

3.3-V to 2.5-V Translation

Figure 1 shows there is enough noise margin (300 mV for low state and 700 mV for high state) to establish reliable translation from 3.3-V logic to 2.5-V logic. This is always valid, but one must ensure that the input clamping diode of the 2.5-V device is not forward biased. V_{IH} should not exceed V_{CC} (2.5-V logic) + 0.3 V.

2.5-V to 3.3-V Translation

Figure 1 shows a 400-mV noise margin for the low-state translation, but zero noise margin for the high state, and therefore, translation from 2.5-V to 3.3-V devices cannot be achieved without additional consideration.

Translating With CBT

A CBT switch is a simple NMOS transistor that acts like a resistor when it is on. Its impedance varies with the amount of current flowing from its drain to its source. A single 3.3-V power supply connected to V_{CC} is not enough to provide sufficient translation since V_{OH} can vary, depending on the input current (I_I) through the switch. The higher I_I is, the lower the output logic level V_{OH} is. A higher 2.5-V device V_{CC} is required to maintain the minimum V_{OH} . The following tables show the required 2.5-V device V_{CC} to maintain a 2-V and 2.4-V V_{OH} .

V _{IN} = 3.3 V, V _{OH(MIN)} = 2 V			
II THROUGH THE SWITCH	REQUIRED V _{CC}		
1 μΑ	2.75 V		
100 µA	3 V		
1 mA	3.1 V		
15 mA	3.5 V		
30 mA	3.7 V		

V _{IN} = 3.3 V, V _{OH(MIN)} = 2.4 V			
II THROUGH THE SWITCH	REQUIRED V _{CC}		
1 μΑ	3.1 V		
100 µA	3.4 V		
1 mA	3.6 V		
15 mA	4 V		
30 mA	4.2 V		

To achieve a good supply voltage to the V_{CC} pin and still be able to modify it based on the input current requirement, a voltage divider should be used to derive the required voltage, as shown in Figure 2. The recommended value of R_2 is 10 k Ω . $C_{(bypass)}$ is the bypass capacitor (recommended value ranges from 0.1 to 0.01 μ F and should be as close as possible to the V_{CC} pin of the CBT device). The value of R_1 is determined from the power-supply voltage, the input current, and the V_{OH} requirement.



Note: $C_{(bypass)} = 0.1$ to 0.01 μ F

Figure 2. Divider Network

Choosing the correct resistor size (R_1) depends on three factors:

- Power-supply voltage level (V_{PS})
- Chip power-supply voltage needed (V_{CC})
- V_{OH} level of the switch

R₁ can be calculated using the generalized formula:

$$R_1 = V_{R1}/I_{R1}$$

Where:

 $\begin{array}{l} v_{R1} = v_{PS} - v_{CC} \\ I_{R1} = I_{R2} + I_{CC} \\ I_{R2} = v_{CC}/R_2 \\ I_{CC} = 100 \ \mu A \\ R_2 = 10 \ k\Omega \end{array}$

The generalized formula for R_1 can be expanded, by substitution, to:

$$R_1 = (V_{PS} - V_{CC})/[(V_{CC}/10 \text{ k}\Omega) + 100 \text{ }\mu\text{A}]$$

(2)

(1)

The following tables show the range of R_1 based on a 5-V supply voltage (V_{PS}), 3.3-V input signal (V_{IH}), 2-V and 2.4-V V_{OH} level with up to 30-mA I_(I) through the switch. These tables allow the designer to choose the correct resistor for the design, based on design requirements.

V _{IN} = 3.3 V, V _{OH(MIN)} = 2 V, I _{CC} = 100 μA					
II THROUGH THE SWITCH	REQUIRED V _{CC} (V)	REQUIRED V _{CC} R ₁ AT V _{PS} = 4.5 V (V) (kΩ)		R ₁ AT V _{PS} = 5.5 V (kΩ)	
1 μΑ	2.75	4.64	6.04	7.32	
100 µA	3	3.74	4.99	6.19	
1 mA	3.1	3.4	4.64	5.9	
15 mA	3.5	2.21	3.32	4.42	
30 mA	3.7	1.69	2.74	3.83	

V _{IN} = 3.3 V, V _{OH(MIN)} = 2.4 V, I _{CC} = 100 μA					
II THROUGH THE SWITCH	REQUIRED V _{CC} (V)	R ₁ AT V _{PS} = 4.5 V (kΩ)	R ₁ AT V _{PS} = 5 V (kΩ)	R ₁ AT V _{PS} = 5.5 V (kΩ)	
1 μΑ	3.1	3.4	4.64	5.9	
100 μA	3.4	2.49	3.65	4.75	
1 mA	3.6	1.96	3.01	4.12	
15 mA	4	1	2	3.01	
30 mA	4.2	0.576	1.54	2.49	

Conclusion

TI's CBT family is versatile, not only in the 5-V or the 3.3-V environment, but also in the 2.5-V arena, using a single 5-V power supply to generate required voltage for its V_{CC} pin. This family functions reliably as long as the above conditions are met.

Acknowledgment

This application report was written by Ramzi Ammar, SLL Applications, Texas Instruments.

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ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading, regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.

EXAMPL	E: SN	74CBT3245A	PW R
Prefix	/		
SN = Standard prefix SNJ = Compliant to MIL-PRF-38535 (QML)	,		
Unique Circuit Description	/		, ,
MUST CONTAIN SIX TO THIRTEEN CHARACTERS			
Examples: 74CBT3125 74CBT16233 74CBTLV162292			
Package ————		/	
MUST CONTAIN ONE TO THREE LETTERS			
D, DW = plastic small-outline package (SOIC) DB, DBQ, DL (or L) = plastic shrink small-outline package (SSOP) [†] DBV = plastic small-outline transistor (SOT) DGG (or G), PW = plastic thin shrink small-outline package (TSSOP) [†] DGV (or V) = plastic thin very small-outline package (TVSOP) [†] FK = leadless ceramic chip carrier (LCCC) JT = ceramic dual-in-line package (CDIP) W, WD = ceramic flat package (CFP) (from pin-connection diagram on individual data sheet)			

Tape-and-Reel Packaging -

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

R = Standard tape and reel [required for DGG (or G) and DGV (or V); optional for D, DL (or L), and DW packages]^{\ddagger}

The purpose of tape-and-reel packing is to position components so they can be placed automatically. Components such as, but not limited to, diodes, capacitors, resistors, transistors, inductors, and integrated circuits can be packed in this manner.

The packing materials include a carrier tape, cover tape, and a reel. The normal dimensions for these items are listed in Table 1.

[†]TI is changing the nomenclature for select logic devices. For details, see page 1–6.

‡ All reeled material previously designated LE will continue to be reeled left embossed, but an R designator will be used.



CARRIER-TAPE WIDTH (mm)	COVER-TAPE WIDTH (mm)	REEL WIDTH (mm)	REEL DIAMETER (mm)
8	5.4	9.0	178
12	9.2	12.4	330
16	13.3	16.4	330
24	21.0	24.4	330
32	25.5	32.4	330
44	37.5	44.4	330
56	49.5	56.4	330

Table 1. Normal Dimensions of Packing Materials

All material meets or exceeds industry guidelines for ESD protection.

Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1,2,3.

Common dimensions of particular interest to the end user are carrier-tape width, pocket pitch, and quantity per reel (see Figure 1 and Table 2).



Figure 1. Typical Carrier-Tape Design



PACKA	AGE	NO. OF PINS	CARRIER-TAPE WIDTH (mm)	POCKET PITCH (mm)	QTY/REEL
SOIC DW	14	16.00	8.00	2500	
	D	16	16.00	8.00	2500
	DW	16	16.00	8.00/12.00	1000
		20	24.00	12.00	1000
SOT	DBV	5	8.00	4.00	3000
301	DCK	5	8.00	4.00	3000
SSOP DB	пр	14/16	16.00	12.00	2000
	υь	20	16.00	12.00	2000
	DL	48	32.00	16.00	1000
	DGG	48	24.00	12.00	2000
TSSOP PV	PW	8	16.00	8.00	2000
		14/16	16.00	8.00	2000
		20	16.00	8.00	2000
TVSOP D	DGV	14	16.00	8.00	2000
		16	16.00	8.00	2000
		20	16.00	8.00	2000
		48	16.00	8.00	2000

Table 2. Selected Tape-and-Reel Specifications



D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150



DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

24–PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-137



DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.C. Body dimensions include mold flash or protrusion.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

24 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. The 24 and 48 pins falls within JEDEC MO-153 and the 14, 16, 20, and 56 pins falls within JEDEC MO-194.



DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



JT (R-GDIP-T**)

24 PIN SHOWN

CERAMIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP-T24, GDIP-T28 and JEDEC MO-058 AA, MO-058 AB.



PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

- D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
- E. Index point is provided on cap for terminal identification only.



CERAMIC DUAL FLATPACK

WD (R-GDFP-F**)





- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for pin identification only

E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA GDFP1-F56 and JEDEC MO-146AB

